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A 3.6 GHz Doherty Power Amplifier with a 40 dBm Saturated Output Power using GaN on SiC HEMT Devices

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by

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Abstract

This manuscript describes the design, development, and implementation of a linear high efficiency power amplifier. The symmetrical Doherty power amplifier utilizes TriQuint's 2nd Generation Gallium Nitride (GaN) on Silicon Carbide (SiC) High Electron Mobility Transistor (HEMT) devices (T1G6001032-SM) for a specified design frequency of 3.6 GHz and saturated output power of 40 dBm. Advanced Design Systems (ADS) simulation software, in conjunction with Modelithic's active and passive device models, were used during the design process and will be evaluated against the final measured results. The use of these device models demonstrate a successful first-pass design, putting less dependence on classical load pull analysis, thereby decreasing the design-cycle time.

The Doherty power amplifier is a load modulated amplifier containing two individual amplifiers and a combiner network which provides an impedance inversion on the path between the two amplifiers. The carrier amplifier is biased for Class-AB operation and works as a conventional linear amplifier. The second amplifier is biased for Class-C operation, and acts as the peaking amplifier that turns on after a certain instantaneous power has been reached. When this power transition is met the carrier amplifier's drain voltage is already approaching saturation. If the input power is further increased, the peaking amplifier modulates the load seen by the carrier amplifier, such that the output power can increase while maintaining a constant drain voltage on the carrier amplifier.

The Doherty power amplifier can improve the efficiency of a power amplifier when the input power is backed-off, making this architecture particularly attractive for high peak-to-average ratio (PAR) environments. The design presented in this manuscript is tuned to achieve maximum linearity at the compromise of the 6dB back-off efficiency in order to maintain a carrier-to-intermodulation ratio greater than 30 dB under a two-tone intermodulation distortion test with 5 MHz tone spacing. Other key figures of merit (FOM) used to evaluate the performance of this design include the power added efficiency (PAE), transducer power gain, scattering parameters, and stability. The final design is tested with a 20 MHz LTE waveform without digital pre-distortion (DPD) to evaluate its linearity reported by its adjacent channel leakage ratio (ACLR).

The dielectric substrate selected for this design is 15 mil Taconic RF35A2 and was selected based on its low losses and performance at microwave frequencies. The dielectric substrate and printed circuit board (PCB) design were also modeled using ADS simulation software, to accurately predict the performance of the Doherty power amplifier. The PCB layout was designed so that it can be mounted to an existing 4” x 4” aluminum heat sink to dissipate the heat generated by the transistors while the part is being driven. The performance of the 3.6 GHz symmetrical Doherty power amplifier was measured in the lab and reported a maximum PAE of 55.1%, and a PAE of 48.5% with the input power backed-off by 6dB. These measured results closely match those reported by design simulations and demonstrate the models’ effectiveness for creating a first-pass functional design.

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I would like to thank all my friends and colleagues at TriQuint who've encouraged me to pursue my academic goals, provided a work environment that supports continued education, and see the personal development of their employees as an investment. Their support has given me the opportunity to engage in research and development outside mobile handset product development engineering and has allowed me to expand my portfolio as an RF design engineer.

I would like to thank Larry Dunleavy and his team at Modelithics who provided TriQuint's 2nd Generation GaN models and passive models. The use of these models saved me several weeks of load-pull characterization, and without them a functional first pass design wouldn't have been possible.

Most importantly I wish to thank my wife, Bernita, who has supported me throughout this entire process. Her encouragement and understanding has helped bring this thesis project to fruition.

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Chapter 1

1.1 Historical Relevance

A new power amplifier technique for amplitude-modulated (AM) radio-frequency signals was introduced by William H. Doherty in 1936. During the time of its inception it represented a more efficient alternative to both conventional amplitude-modulated techniques and Chireix outphasing. [1,2]. This technique achieves higher plate efficiencies, up to 65% independent of modulation, by means of a combined action of the variation of load distribution of the vacuum tubes, and the variation of the circuit impedance over the modulation cycle. When Doherty joined the Bell Telephone Laboratories in June 1929, he was engaged in the development of high-power radio transmitters for transoceanic radiotelephony and broadcasting. This led to a breakthrough to greatly improve the efficiency of radio-frequency power amplifiers which is now ubiquitously termed the “Doherty amplifier”. The Doherty amplifier was first used in a 50 kW transmitter application with low audio frequency distortion of less than a few percent. These amplifiers operated with an efficiency of 60%, representing a reduction of nearly one-half the power consumption compared to a conventional linear amplifier operating at 33% efficiency [3].

In the years that followed, Doherty amplifiers continued to be used in a number of medium and high power low-frequency (LF) and medium-frequency (MF) vacuum tube AM transmitters [4,5]. A one-megawatt AM transmitter operating in the long-wave band began regular operations in postwar Europe in August 1953, where the outputs of two 500 kW Doherty amplifiers were joined in

a bridge configuration. The practical implementation of classical triode-based Doherty scheme was restricted by its substantial nonlinearity for both linear amplification of AM signals and grid-type signal modulation that required complicated envelope correction and feedback linearization circuits. However, Doherty amplifiers employing tetrode transmitting tubes could improve their overall performance when the modulation was applied to screen grids of both the carrier and peaking tubes, while the control grids of both tubes are fed by a nearly constant level of RF excitation. This resulted in the peaking tube being modulated upward during the positive half of the modulating cycle and the carrier tube being modulated downward during the negative half of the modulating cycle [6].

For the classical Doherty power amplifier with matched power tubes, the transition voltage is half the peak-envelope power (PEP), and the total output power of the amplifier comes from the carrier tube for input amplitudes less or equal to the transition point. The region between the transition point and PEP values represents the load modulation region and the voltage of the carrier tube remains constant at the PEP level. The voltage seen at the peaking tubes continues to rise linearly, with its current rising twice as fast as the current in the carrier tube in order to reach its PEP value at maximum output power. Therefore, at low output power levels, the carrier amplifier operates linearly, reaching saturation that corresponds to maximum efficiency at some transition voltage below the system peak output voltage. However, in the presence of

higher output power levels the carrier amplifier remains saturated while the peaking amplifier operates linearly.

1.2 Overview

This manuscript describes the design, development, and implementation of a linear high efficiency power amplifier. The symmetrical Doherty power amplifier utilizes TriQuint's 2nd Generation 2.5 mm GaN HEMT devices (T1G6001032-SM) for a specified design frequency of 3.6 GHz and saturated output power of 40 dBm. Advanced Design Systems (ADS) simulation software, in conjunction with Modelithic's active and passive device models, are used throughout the design process and will be evaluated against the final measured results. The omission of classical load-pull analysis represents a potential reduction in design-cycle times, enabling a designer to get their product to market faster.

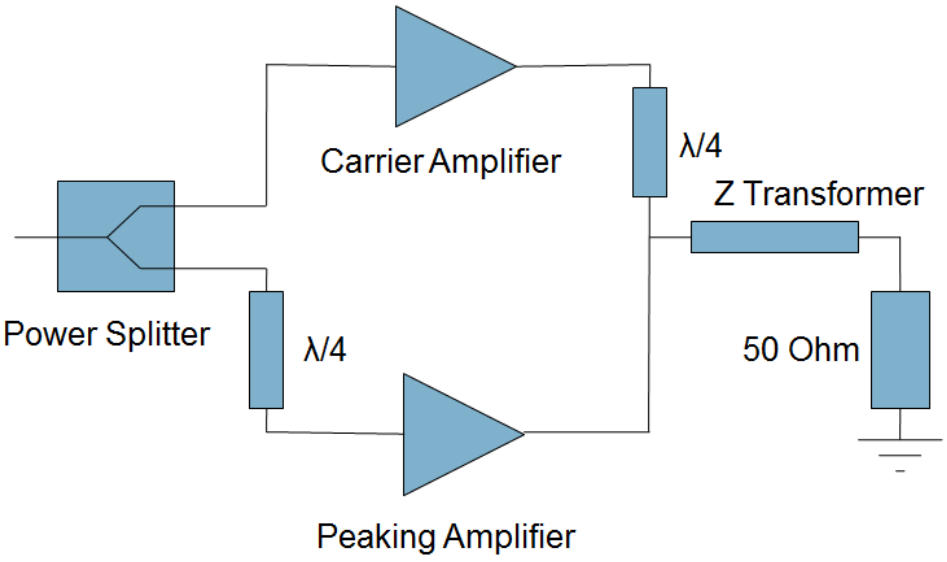


Figure 1: Block Diagram of Doherty Power Amplifier [7]

A functional block diagram of a symmetric Doherty power amplifier is shown in Figure 1. The RF input signal passes through a power splitter where the power is equally split, implying a 3 dB drop in output power at the output of the splitter. The RF input signal feeding the peaking amplifier is then passed through a quarter-wavelength transformer which inverts the impedance between the carrier and peaking transistor. A more cost-effective way to achieve the function of the power splitter and quarter-wavelength transformer is by employing a 90 degree 3 dB hybrid coupler. These devices can be realized in very small packages with a low temperature co-fired ceramic (LTCC). At the output of the carrier amplifier a quarter-wavelength transformer recombines the output signal of the carrier and peaking amplifier. From this node the modulated impedance is approximately half that of the 50 ohm system impedance. Thus, a quarter-wavelength transformer is employed to convert the modulated impedance to the system impedance, ensuring the maximum power transfer to the load is being satisfied.

The carrier amplifier works as a conventional linear amplifier and is usually biased in Class-AB. The second transistor acts as the peaking amplifier and is controlled in a way that it turns on only after a certain instantaneous power has been reached. In the classical design of Doherty power amplifiers the peaking amplifier is typically biased for Class-C operation. When this power transition is met the carrier amplifier's drain voltage is already approaching saturation, if the input power is further increased, the peaking amplifier modulates the load seen by the carrier amplifier, such that the output power can increase while

maintaining the drain voltage level of the main amp constant. This results in an amplifier that maintains high efficiency throughout the load modulation region depicted in Figure 2.

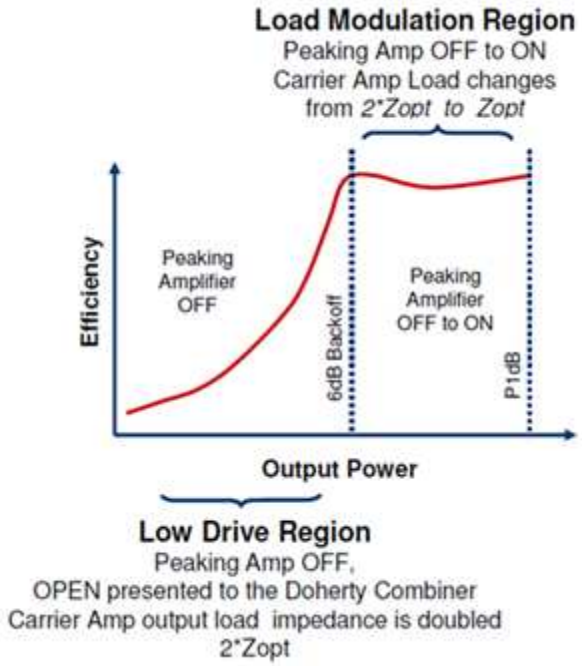


Figure 2: Characteristic Efficiency of a Doherty Power Amplifier [7]

The concept of a load modulated power amplifier can be viewed as an active load-pull technique, where the reactance of the RF load can be modulated by applying current from a second phase coherent source. Referring to Figure 3, the source on the left "sees" a load resistance of R_L, if the generator on the right sources a zero current. However, if both the sources are supplying current, both currents flow into the load resistor such that the voltage appearing across the load resistance can be calculated using the following equation.

$$V_L = R_L \left(I_1 + I_2 \right) \tag{1.1}$$

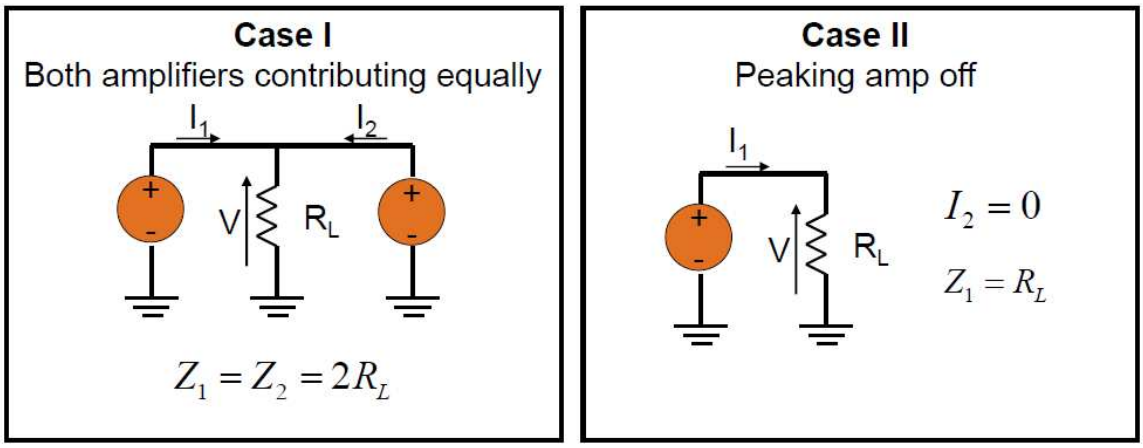


Figure 3: Impedance cases for Doherty Power Amplifier [8]

This can be applied to AC circuits if complex notation is used to represent magnitude and phase of the voltages and currents and the resistive and reactive components of the impedances. In this form, the equations show the possibility of changing, or "pulling" the impedance seen by source on the left by controlling the magnitude and phase of the current I_2 [8].

$$Z_1 = R_L \left(1 + \frac{I_2}{I_1} \right) \tag{1.2}$$

Balanced amplifiers are combined in parallel with the assumption that the impedance seen by each has some common load impedance scaled up by the number of parallel devices. It assumes that the devices are identical in terms of device periphery, bias, and drive level. For the design of Doherty power amplifiers these conditions can be relaxed so that the impedance seen by each element is a function of other elements as well as the common load.

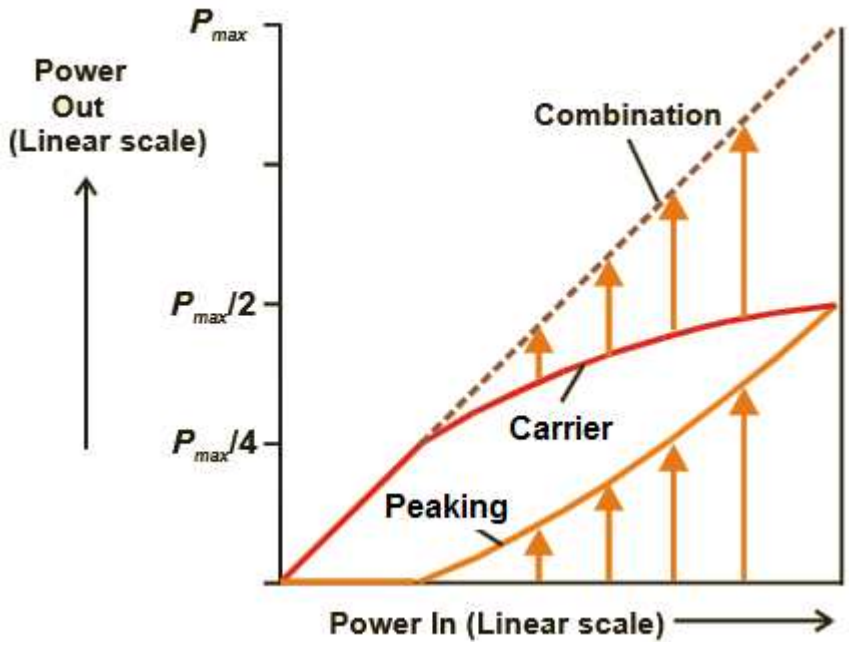


Figure 4: Carrier and Peaking Amplifier Power Contributions [8]

The RF output power of a Doherty power amplifier is a combination of the carrier and peaking amplifier which is depicted in Figure 4. As the input power is increased from small-signal to large-signal, only the carrier amplifier is functioning and the peaking amplifier is in an non-active state. When a certain instantaneous RF input power is reached the peaking amplifier begins to contribute to the output power. The key action of the Doherty power amplifier occurs during the region where the peaking device is active and the main device is held in a constant maximum voltage condition. This is achieved thorough the dynamic resistance of the load whose effective value decreases dynamically with increasing drive level due to the load-pulling effect of the peaking amplifier, thereby maintaining maximum voltage swing and high efficiency. The output power increases in proportion to the input voltage drive level, so that a square

root characteristic is observed by the carrier amplifier. The peaking amplifier produces an upward load-pull effect, so that it generates an output power proportional to the cube of the increasing input voltage amplitude. In theory, these two characteristics combine to produce a composite linear power response [8].

The design presented in this manuscript was tuned to achieve maximum linearity trading-off its maximum PAE and 6dB backed-off PAE, in order to maintain a carrier-to-intermodulation ratio greater than 30 dB when excited by two-tones with 5 MHz tone spacing. The load modulation characteristic is much softer than in an ideal, symmetric Doherty power amplifier, which suggests that the carrier amplifier's drain voltage is not saturated at the onset of load modulation. Although this design strategy does not lead to the efficiency characteristic of an ideal Doherty power amplifier, it offers a significant boost in average efficiency compared to a Class AB design.

The use of modulated carriers for the down link in mobile telecommunication systems contain high peak power signal characteristics but on average operate at much lower power levels. A single-ended Class AB PA is very inefficient with a high peak to average signal. The power amplifier needs to be sufficiently large to meet the peak output requirements while maintaining efficiency at lower power levels when backed-off considerably from saturation. This can be performed with Doherty power amplifiers by improving the efficiency and operating under dynamic load conditions.

The demand for linear high efficiency power amplifiers in small-cell base station applications are required to support the increasing data rates for modulations such as Orthogonal Frequency Division Multiplexing (OFDM), which is used predominately in Long Term Evolution (LTE) 4G networks. Typically, the use of digital pre-distortion (DPD) is required to reduce the distortion mechanisms cause by AM-AM, AM-PM, and memory effects. The motivation for using a symmetrical Doherty power amplifier using GaN on SiC HEMT devices are its high efficiency, lower operating expenses, lower capital expenditures, and smaller size. The lower capital expenditure is largely due to the cost reduction of the power supplies, reduced heat dissipation requirements, and overall reduction in mass. Moreover the Doherty power amplifier is a proven architecture with adequate bandwidth to meet today's telecommunication standards [6-9].

Chapter 2
Amplifier Characteristics Overview

2.1 Classes of Operation

There are numerous texts and papers dedicated to the performance characteristics of power amplifiers [6] – [15], and in this chapter an overview will be presented. Typically, power amplifiers can be distinguished from one another by their class of operation. There are several classes of operation denoted by the amplifiers voltage and current waveforms. These classes are generally defined by four criteria: efficiency, power, linearity, and conduction angle.

Efficiency is defined as the ratio of the Radio Frequency (RF) power to the Direct Current (DC) power. Power is the capability of delivering a voltage or current to the amplifier's load at the frequency of interest. The conduction angle is considered 100% when the device is always on and the waveforms are not distorted. To a lesser degree the biasing and matching networks provided to the amplifier also help to define what class of operation the amplifier performs in. Table 1 summarizes the qualities of amplifiers operating in different classes of operation.

Table 1: Summary of Amplifier Class of Operations [10]

Class	Efficiency	Power	Linearity	Conduction Angle
A	25% Max.	High	Best	100%
AB	< 68%	High	Some Distortion	< 100%
B	78.5% Max.	High	More Distortion	50%
C	> 78.5%	Low	Poor	< 50%
D	< 100%	Medium	Moderate	50%
E/F	100%	Low	Poor	50%

The performance of the symmetric Doherty power amplifier can be described by Figures of Merit (FOM). These include the maximum output power, one decibel (1 dB) compression point, Third-Order Intercept (TOI), stability, bandwidth, etc. An overview of these FOM will be provided in this chapter giving a thorough treatment for each.

2.1.1 CLASS-A

The classic defining behavior of a Class-A power amplifier is its linearity. Figure 5 illustrates that the Class-A power amplifier can amplify a signal while maintaining its linear transfer characteristic with no distortion. However, Class-A power amplifiers are horrendously inefficient and can only achieve a theoretical 25% efficiency when capacitive-coupled to the load. In a power amplifier, this not only wastes power but potentially increases the operating costs. This inefficiency comes from the standing current, approximately half the maximum output current, and a large part of the power supply voltage present across the output of the device at low signal levels.

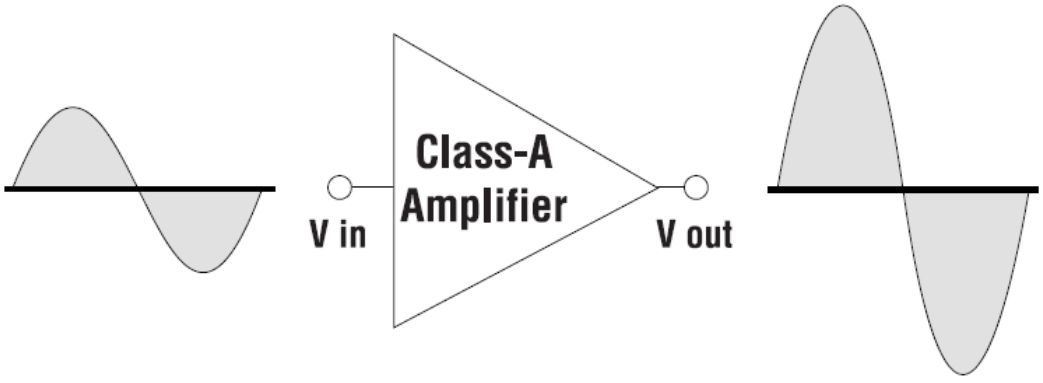


Figure 5: Linear Operation of Class-A Amplifier [10]

The typical single-stage amplifier employing a common cathode/emitter/source configuration inverts the phase of the signal but maintains a constant gain associated with the power entering the device. In order to maintain a linear response, the input power level applied to a Class-A power amplifier must be relatively small. This prevents the amplifier from being overdriven, which in turn prevents the amplifiers output from reaching saturation. The load line technique is a common method used to design Class-A amplifiers to ensure the device is appropriately biased to achieve a linear output. A graphical depiction of the load line technique for biasing a device is shown in Figure 6.

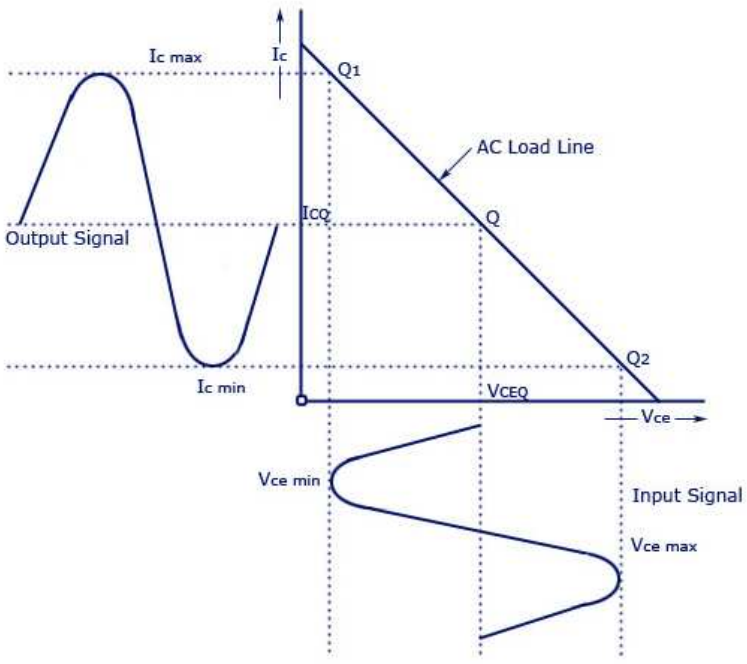


Figure 6: Graphical Depiction of Load Line Technique for Biasing Device [10]

The waveform of the collector or drain current is biased at a level greater than the amplitude of the input signal current in order to maintain linear

operation. The conduction angle is said to be 100% because current flows during the whole waveform period and maintains a sinusoidal output as seen in Figure 7.

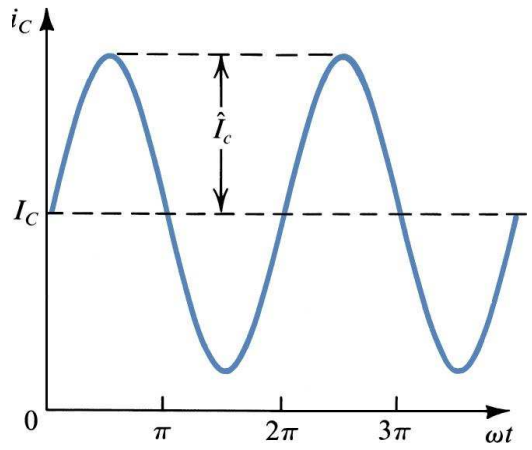


Figure 7: Collector/Drain Current Waveform for Class-A [10]

2.1.2 CLASS-B

When a device operates as a Class-B amplifier, the most obvious contrast is evident in the collector/drain or emitter/source current waveforms where the conduction angle is now 50%. The DC supply is reduced by a factor of 2/π compared to the class A condition, resulting in a theoretical efficiency of π/4 or about 78.5%. This is shown in Figure 8 where the device will conduct current only half the time while being in an off condition the other half. The device is biased in such a way that the signal current is the only source to turn on the device and the DC bias current is nearly zero. When the base drive signal voltage falls below a certain level, the transistor collector current vanishes and the transistor is “Off.” It is also evident that the signal being amplified will have more distortion compared to the Class-A power amplifier.

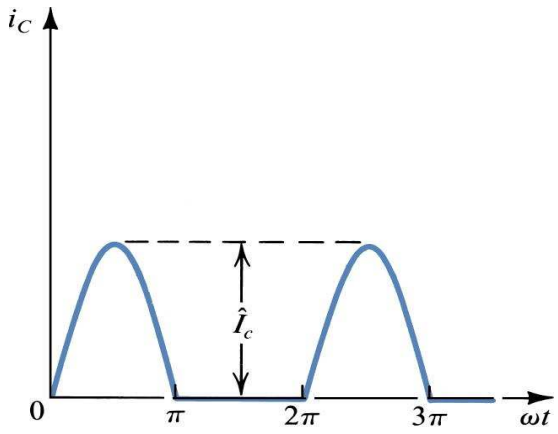


Figure 8: Collector/Drain Current Waveform for Class-B Operation [10]

The downside is that in theory 6 dB more drive power is needed to achieve the Class B condition. The upside is that Class-B linearity is improved under 3 dB backed-off conditions. Due to the symmetry of the drive signal about the pinch-off level, the conduction angle remains constant for varying drive levels. Therefore, a 3 dB reduction in input power corresponds to a 3 dB reduction in output power, demonstrating its linear behavior. At this drive level the efficiency could be increased by increasing the load resistor value which results in larger voltage swing.

Practical implementations of Class-B amplifiers in push-pull configurations sometimes experience a slightly reduced conduction angle over the theoretical Class-B operations. This occurs when the transistors are operated at a zero voltage base (BJT) or gate (MOS) bias. This causes crossover distortion where both transistors in the push-pull configuration are in the “off” state. As in the single-ended Class-B operations the maximum theoretical efficiency is 78.5%,

but comes with the added benefit of cancelling even harmonic distortion products.

2.1.3 CLASS-AB

A compromise between Class-A and Class-B operation is referred to an amplifier classification known as Class-AB. In Class-AB operation the device operates over half the waveform the same way as in Class-B operation, but also conducts a small amount of current on the other half. The device is biased at a non-zero DC current where the magnitude of the current is dictated by the trade-off between linearity, efficiency, and power. The bias point selected determines the voltage swing and the conduction angle which can be seen in Figure 9.

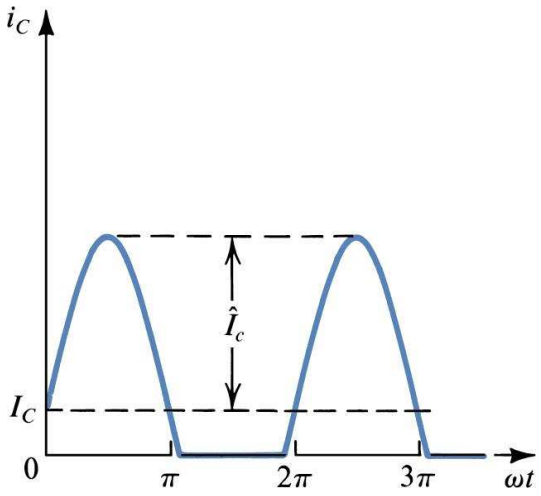


Figure 9: Collector/Drain Current Waveform for Class-AB Operation [10]

A significant reduction in the DC component of the device current results in an increased theoretical efficiency of 68%. However, these effects only come at the expense of input drive power, which constitutes a reduction in overall power gain when compared to a Class-A power amplifier. One important issue

that is often overlooked in Class-AB operation is the effect of a 3 dB reduction in drive level. Unlike the Class-A case, the output power does not show a corresponding 3 dB drop. This implies that the amplifier is a non-linear amplifier where a signal with an amplitude-modulated envelope will be distorted at peak power levels [8].

2.1.4 CLASS-C

Operations under Class-C conditions occur when the output tuning network conditions the signal, typically through a parallel resonant inductor capacitor (LC) circuit. This resonant circuit is tuned to the frequency of interest and sustains the RF waveform during the non-conducting part of the cycle. The non-conducting portion of the cycle can be seen in Figure 10. Typically, the output matching is a parallel resonant circuit that is designed to provide an output signal that is proportional to the input signal at the resonant frequency of interest.

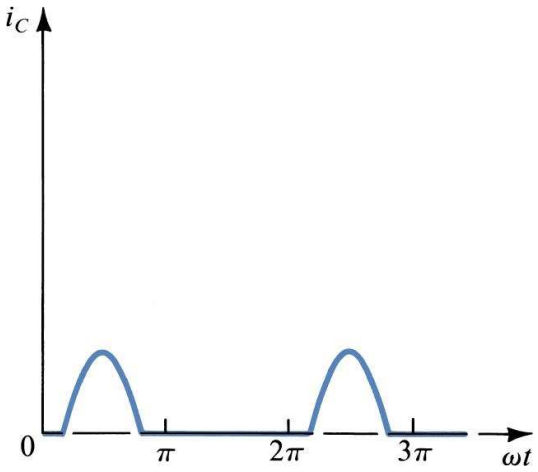


Figure 10: Collector Current Waveform for Class-C Operation [10]

The current waveform starts to take an appearance of series of short pulses, having a low DC component, and also a lower fundamental component in comparison to Class-AB. Very high efficiency can be achieved, but it comes with the burden of heavy input drive requirements, a reduction in maximum output power, and a reduction in linearity.

2.2 Figures of Merit

Besides amplifiers being described by their class of operation, they are also described by Figures of Merit (FOM). Generally speaking the FOM characteristics are based on the performance of the amplifier under specific test and measurement conditions. Thus these specified conditions need to be well documented and held stable for the measurement to accurately compare the strengths or weaknesses of the device under test (DUT). The following FOM's are used:

- Power-Added-Efficiency
- Output referred third-order intercept point
- 1-dB compression point
- Maximum Output Power
- Stability
- Transducer Power Gain
- Matching Technique
- Scattering Parameters

2.2.1 POWER-ADDED-EFFICIENCY

Power-Added-Efficiency (PAE) is a measure of a device's ability to convert the applied DC power to an RF power for a given fundamental frequency. Calculating PAE accounts for the input power (P_{RFin}) to the device as shown in Equation 2.1.

$$PAE = \frac{P_{RFout} - P_{RFin}}{P_{DC}} = \frac{P_{RFout} - P_{RFin}}{V_{DC} \text{ x } I_{DC}} \tag{2.1}$$

For devices where there is low to moderate gain the inclusion of the RF input power can be significant. PAE is the most accepted FOM when comparing the efficiency of devices. PAE differs from drain efficiency in that drain efficiency measures how much DC power is converted to RF power. The problem with using this measurement is that it does not take into account the incident RF power that goes into the device. This can be substantial in a single-stage RF device where gain is low.

2.2.2 OUTPUT THIRD-ORDER INTERCEPT POINT

While the output third order intercept (TOI) point is not directly measured in devices with good linearity, it is used to assess the distortion products of the device. It is an indicator of the intermodulation distortion (IMD) that exists in non-linear systems. Please recall the trigonometric identity where two cosines are summed together to create the sum and difference frequencies.

$$\cos(x)\cdot\cos(y) = \frac{1}{2}\left[\cos(x-y) - \cos(x+y)\right] \tag{2.2}$$

Not only are the sum in difference frequencies created but the higher order harmonic frequencies are generated as well. Figure 11 demonstrates how a two-tone IMD test can be used to determine the value of the third-order IMD products.

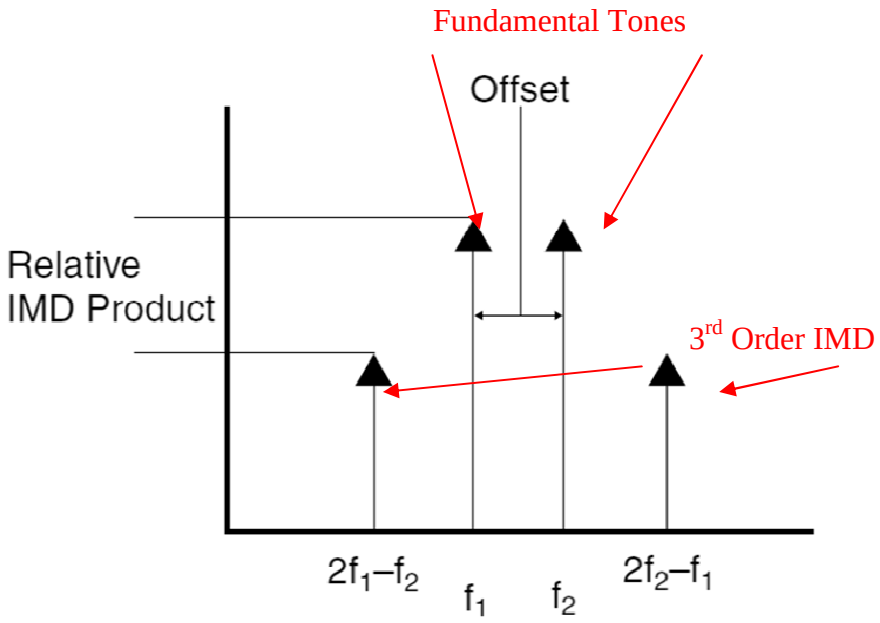


Figure 11: Frequency Graph of a Two-Tone Measurement [10]

The third order IMD product will increase in magnitude as the input power of the fundamental tones increase. This increase will depend upon the offset spacing and the gain of the device at the frequencies used, but a general rule of thumb is for every 1 dB of increased input power, there will be a 3 dB increase to third-order IMD products. The output third-order intercept refers to the output power where the output power and 3-order IMD power are extrapolated beyond their linear region and intersect at a single-point.

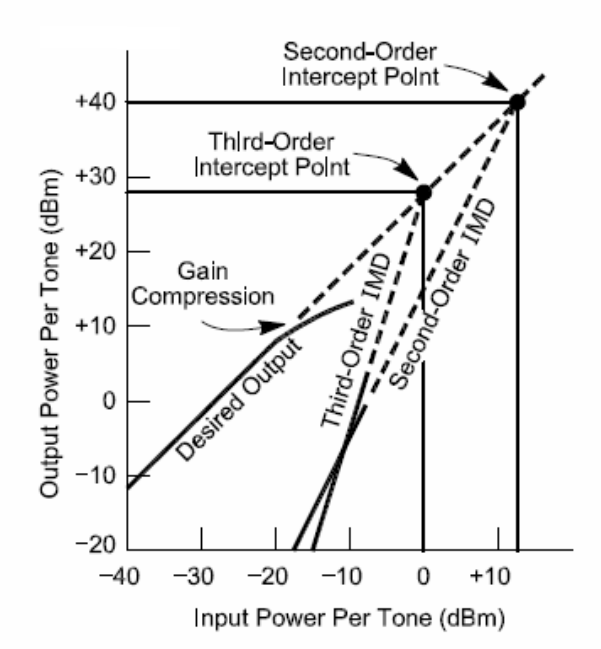


Figure 12: P_{out} versus P_{in} Graph Illustrating Intercept Points [10]

The information gained from a power amplifier operating in the linear region is helpful in identifying the characteristics and behavior. This information is also used to extrapolate into other FOM parameters. As can be seen in Figure 12 there are several characteristics of the DUT that can be extracted from a Pout versus Pin graph. In general, linearization itself leads to better efficiency and applies to real-world linear power amplifiers, where a certain level of linearity is mandatory.

2.2.3 1dB COMPRESSION POINT

The 1dB compression point is defined by extrapolating the linear gain curve beyond its measured saturation region and determining the point where the measured gain is 1 dB below the extrapolated linear gain point, as shown in Figure 13.

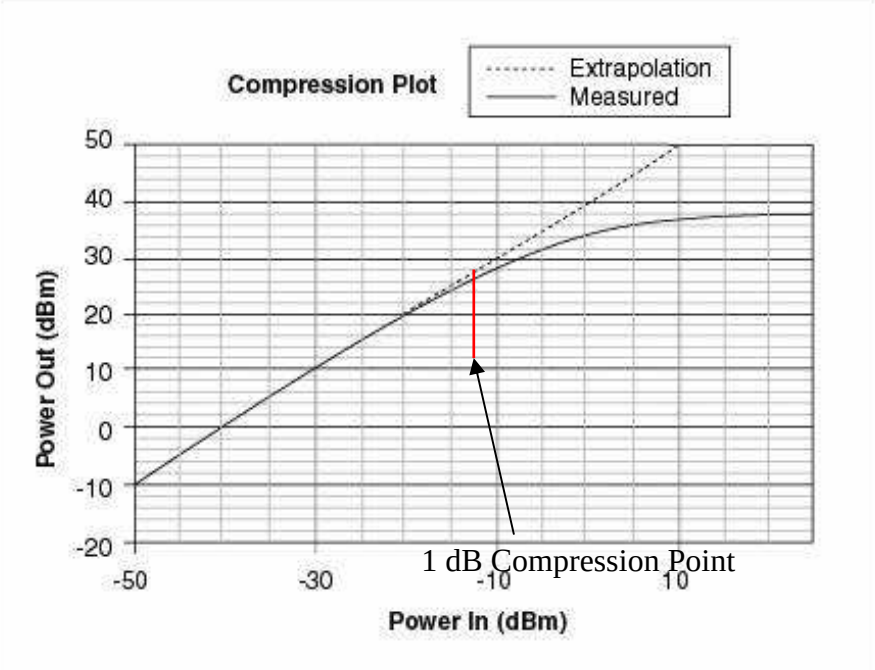


Figure 13: Measured and Extrapolated Gain Compression Plot of an Amplifier [10]

Other compression points such as 0.5 dB and up to 2 and 3 dB can be determined in the same manner as necessary up to where the amplifier is fully saturated.

2.2.4 MAXIMUM OUTPUT POWER

The maximum output power region is where the device is saturated and the device cannot output any additional power into the load. This condition is generally where the efficiency of the device is high and the output voltage is severely clipped, as shown in Figure 14. The graph shows what the ideal output waveform may look like compared to the saturated condition.

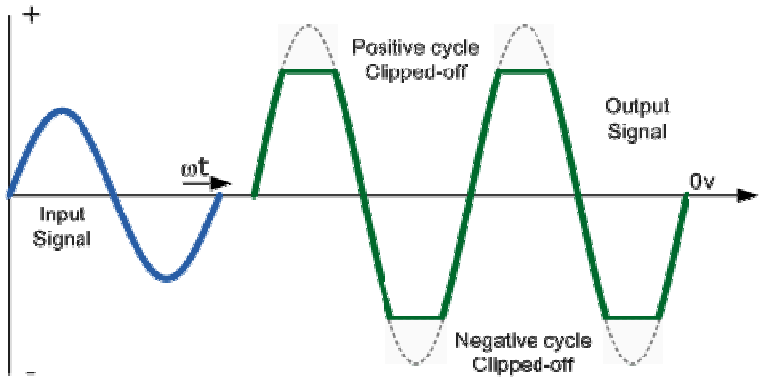


Figure 14: Ideal Waveform Compared to Compressed Amplifier Output [10]

2.2.5 STABILITY

The stability of a device is one of the key elements to a successful design and demonstrates an amplifier's resistance to oscillate. In a two-port network, oscillations are possible when either the input or output presents a negative resistance. This occurs when either $|S_{11}|$ or $|S_{22}|$ are greater than one. A device is said to be unconditionally stable at a given frequency if the real parts Z_{in} and Z_{out} are greater than zero for all passive load and source impedances [16]. The traditionally accepted equation to determine unconditional stability is the Rollet condition, where if *K* is greater than one the device meets the requirements to be unconditionally stable. This can be determined by 2-port S-parameter data from the equation below.

$$K = \frac{1-|S_{11}|^2-|S_{22}|^2+|\Delta|^2}{2|S_{21}S_{12}|} > 1, \qquad where\ \Delta = S_{11}S_{22} - S_{12}S_{21} \qquad (2.3)$$

2.2.6 TRANSDUCER POWER GAIN

The transducer power gain of device is defined as the power delivered to the load at the fundamental frequency (dBm), minus the power available from the source (dBm). The transducer power gain eliminates the issue of negative insertion loss, where a passive network might increase delivered power [17]. Transducer power gain is the decibel ratio of power delivered to the load to the power available from the source.

$$TransducerGain = 10\log\frac{P_L}{P_A} \tag{2.4}$$

2.2.7 BANDWIDTH

The bandwidth of a device describes how much spectrum a system is capable of responding to, and can be quantified in a variety of ways depending on the specific system requirements. The 1-dB bandwidth can be defined where the transmission coefficient S_{21}, falls off from its highest peak by 1-dB from its high frequency, F_h, to low frequency, F_l. In a similar manner the 2-dB and 3-dB bandwidths can be found. Another way to define bandwidth is the percentage bandwidth of a system. It can be found by determining the difference between the high frequency F_h, and low frequency $F_{L,}$ divided by it center frequency, F_c, and multiplied by 100%. Similarly, the transmission coefficient can be defined the case where S_{21} falls *by* 1, 2, or 3dB from its center frequency.

$$BW(\%) = \frac{F_h - F_l}{F_c} \cdot 100\% \tag{2.5}$$

2.2.8 MATCHING TECHNIQUE

The input and output matching of any power amplifier is of utmost importance to the performance of the device. To obtain the maximum power transfer, we must transform characteristic impedance, Zo, from the source to the complex input impedance seen looking into the transistor, Zs. Similarly, we must transform the complex output impedance, $Z_{L,}$ looking into the output of the transistor to the Zo of the load.

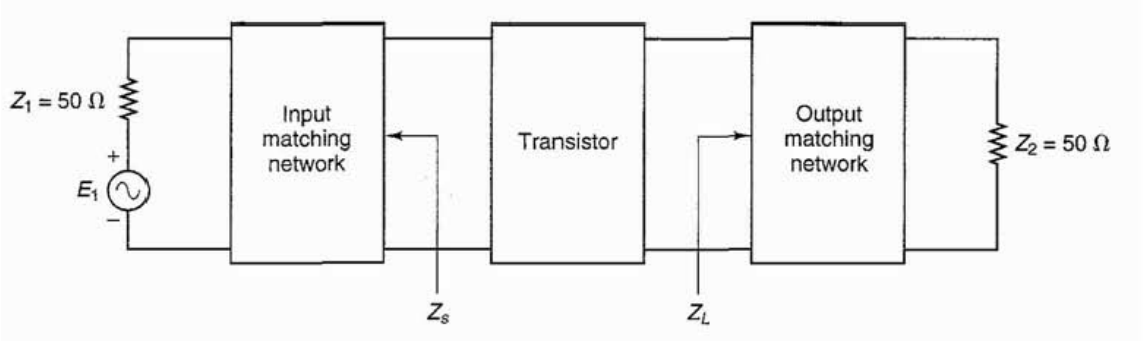


Figure 15: Block Diagram of Microwave Amplifier [16]

A number of techniques can be used to design input and output matching networks. Because the relatively high 3.6 GHz design frequency and the performance of most lumped components at these frequencies a transmission line, TL, technique on microstrip was selected to perform the input and output matching of the device.

2.2.9 S-PARAMETERS

The scattering parameters, commonly referred to as S-parameters, give a complete description of the network as seen at its *N*-port network. The scattering matrix relates the voltage wave incident on the port to those reflected from the port [18]. S-parameters can be calculated using network analysis techniques or measured on a Vector Network Analyzer (VNA) like that shown in Figure 16.

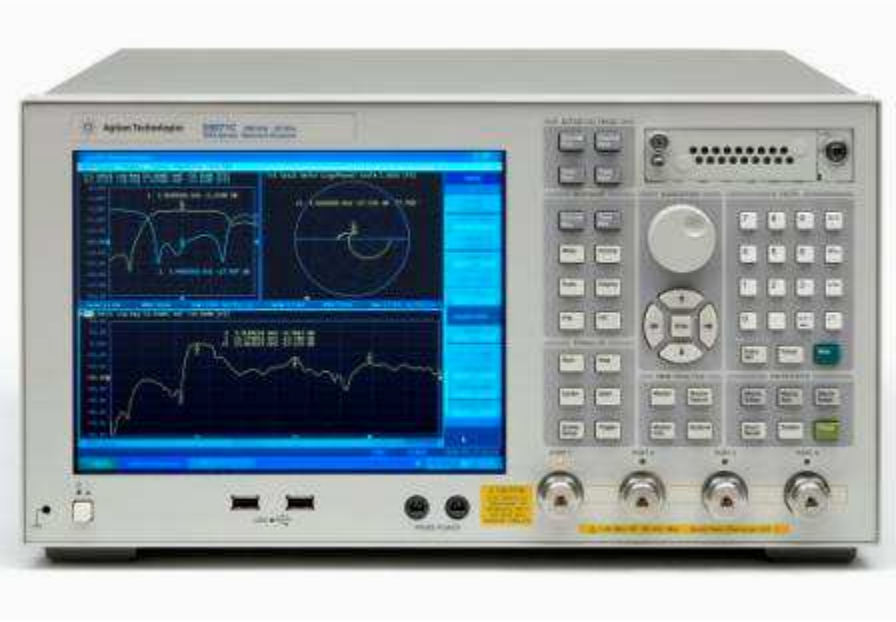


Figure 16: Agilent ENA E5071C Vector Network Analyzer

Consider the two port network shown in Figure 17, where V_n^+ is the amplitude of the voltage wave incident on port *n,* and V_n^- is the amplitude of the voltage wave reflected from port *n.* The scattering matrix, [S] is defined in relation to those incident and reflected voltage wave.

$$[S] = \begin{bmatrix} V_1^- \\ V_2^- \end{bmatrix} = \begin{bmatrix} S_{11,} S_{12} \\ S_{21,} S_{22} \end{bmatrix} \begin{bmatrix} V_1^+ \\ V_2^+ \end{bmatrix} \tag{2.6}$$

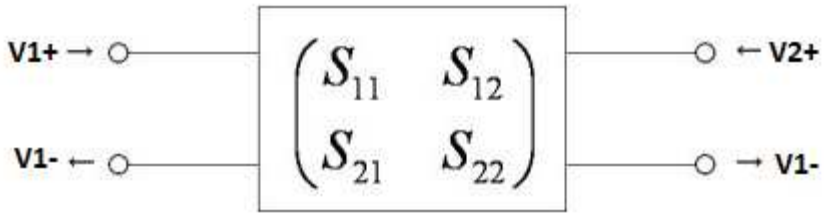


Figure 17: Agilent ENA E5071C Vector Network Analyzer

The first number of the subscript refers to the measured port, while the second number refers to the incident port. For example, $S_{21,}$ means the response at port 2 due to a signal at port 1. By applying a signal to port 1 with an incident wave of voltage, V_1^+, and measuring the reflected wave amplitude, V_2^-, coming out of port 2. This assumes that all ports are terminated in matched loads, *Zo*, to avoid reflections except for port 1. Therefore, S_{11}, is the reflection coefficient seen looking into port 1, when all other ports are terminated in matched loads, and S12 is the transmission coefficient from port 2 to port 1 when all other ports are terminated in matched loads. If we assume that each port is terminated in impedance *Zo*, we can determine the four S-parameters of the two-port network by equation (2.7).

$$S_{11} = \frac{V_1^+}{V_1^-} \qquad S_{21} = \frac{V_2^-}{V_1^+}$$

$$S_{12} = \frac{V_1^-}{V_2^+} \qquad S_{22} = \frac{V_2^-}{V_2^+} \tag{2.7}$$

S-parameters can be presented in one of two ways, linear magnitude or quantified logarithmically in decibels (dB). The latter being the more commonly used quantification found in industry. Because S-parameters are a voltage ratio, and power is proportional to voltage squared, the formula to convert the linear magnitude to decibels can be found using equation (2.8).

$$S_{ij}(dB) = 20 \cdot \log\left|S_{ij}\right| \tag{2.8}$$

2.2.10 PEAK-TO-AVERAGE RATIO

The peak-to-average ratio (PAR) is the ratio of the peak power level to the time average power level. The PAR can be represented as a ratio of the statistical occurrence of a peak relative to an average power level. The peak power of the PAR is often defined as 0.01% complementary cumulative distribution function (CCDF). Figure 18 shows an example of the CCDF for a typical QPSK and OCQPSK signal with a resolution bandwidth of 5MHz.

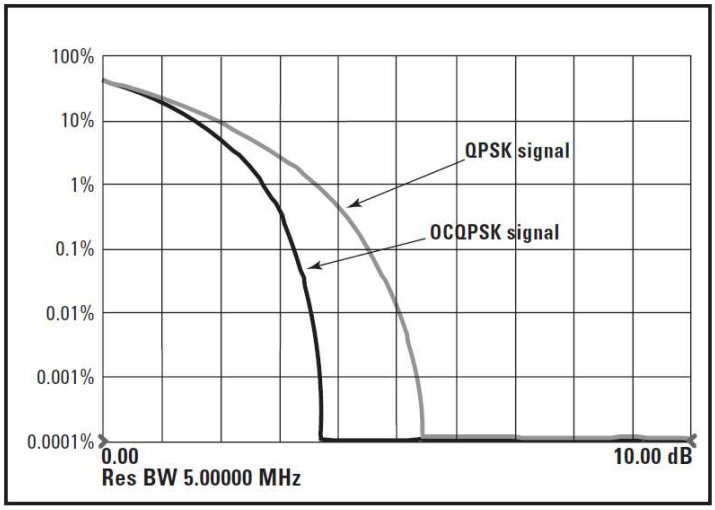


Figure 18: PAR of QPSK and OCQPSK signal [7]

Chapter 3

Semiconductor Process, Device, and Model Overview

3.1 Semiconductor Technology

The TriQuint T1G6001032-SM is a 10 Watt (P3dB) discrete GaN on SiC HEMT device which operates from DC to 6 GHz. The device was designed using TriQuint's TQGAN25 production process, a high-frequency 0.25 micron GaN on SiC. This process features advanced field plating techniques to optimize microwave power and efficiency at high drain bias operating conditions. This optimization can potentially lower system costs in terms of fewer amplifier line-ups and lower thermal management costs. This 2nd Generation GaN brings reliable integrated RF solutions that use less power, are compact, and serve wide frequency ranges. The TQGAN25 process supports frequencies from DC to 18 GHz including discrete transistors, MMICs, and packages solutions. TriQuint's TQGAN25 process can operate up to 40 Volts and has achieved a mean time to failure (MTTF) of greater than 10 million hours at 200℃ and greater than 1 million hours at 225℃.

3.2 Transistor Performance

The symmetric Doherty power amplifier utilizes two of TriQuint's T1G6001032-SM GaN on SiC HEMT operating from DC to 6 GHz. This optimization can potentially lower system costs in terms of fewer amplifier line-ups and lower thermal management cost [19]. The functional block diagram for the T1G601032-SM GaN Packaged transistor is shown in Figure 19.

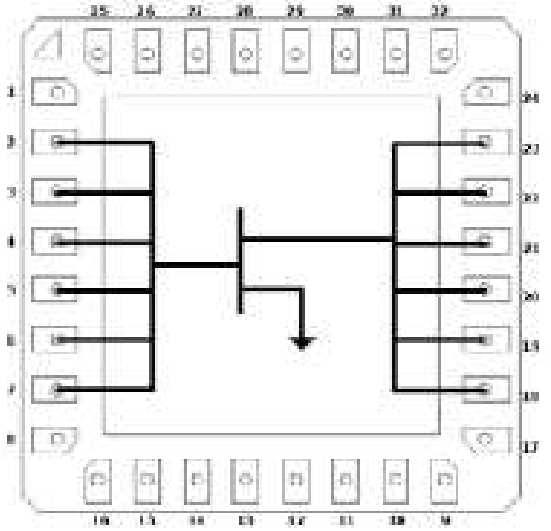


Figure 19: Functional block diagram for T1G6001032-SM [19]

The transistors absolute maximum ratings are provided in table 2 below. The operation of this device outside the parameter ranges may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not recommended.

Table 2: Absolute Maximum Rating [19]

Parameter	**Value**
Breakdown Voltage (BV_{DG})	100 V (Min)
Gate Voltage Range ($V_{G)}$	-7 to 0 V
Drain Current (I_D)	1.2 A
Gate Current ($I_{G)}$	-2.5 to 4.2 mA
Power Dissipation (P_D)	16 W
RF Input Power, CW, T = 25 deg C (P_{IN})	34 dBm
Channel Temperature (T_{CH})	275°C
Mounting Temperature (30 Seconds)	320°C
Storage Temperature	-40 to 150°C

The recommended operating conditions for the T1G6001032-SM transistor is provided in table 3.

Table 3: Recommended Operating Conditions [19]

Parameter	Value
Drain Voltage (V_D)	32 V
Drain Quiescent Current (I_{DQ})	50 mA
Peak Drain Current (I_D)	650 mA
Gate Voltage (V_G)	-2.9V
Channel Temperature (T_{CH})	225°C (Max)
Power Dissipation, CW (P_D)	11.8 W (Max)
Power Dissipation, Pulse (P_D)	12.5 W (Max)

3.3 Transistor Model

The HMT-TQT-T1G6001032-SM-001 is a nonlinear model created by Modelithics for TriQuint's T1G6001032-SM packaged GaN transistor. The model is based on the extraction of a customized Angelov nonlinear model that is validated against I-V, S-parameters, and large signal load pull measurement datasets. The model is extracted such that performance can be scaled with temperature and quiescent bias voltage. The model representation for HMT-TQT-T1G6001032-SM-001 is shown in Figure 20 [20].

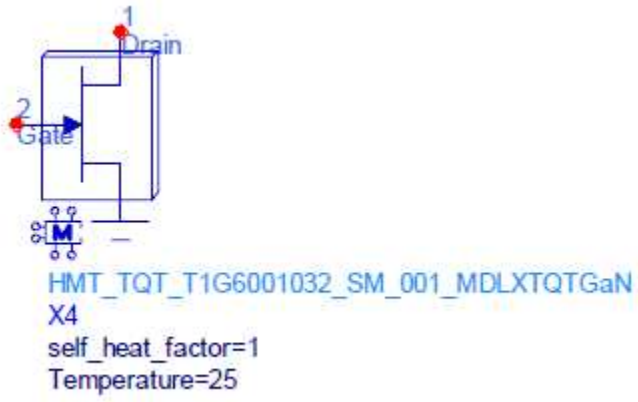


Figure 20: HMT-TQT_T1G6001032-SM-001 Model Representation [20]

The model is optimized for operation for V_{DD} equal to 32 V. The model parameter, *temperature,* represents the backside ambient temperature. The model parameter, *self_heat,* is a scaling factor for the electro-thermal model (range from 0 to 1), 0 = self-heating is turned off, 1(default) = self-heating is fully turned on, and a value of 0.1 is representative of 10% thermal duty cycle. The device was characterized on a Zo = 50 ohm test fixture to set the reference planes at the edge of the ceramic package as shown below in Figure 21 [20].

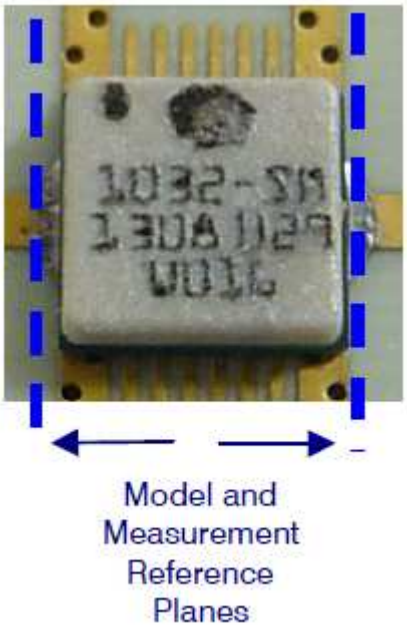


Figure 21: Model and Measurement Reference Plane [20]

The desired IV characteristics call for a V_{DD} of 32V and an idle quiescent current of 50mA. The vendor's models pulsed IV characteristics are shown in Figure 22, where the voltage gate to source (V_{gs}) is swept from -4V to 0.V in 0.2V increments with measurement pulse width of 0.5 microseconds equal to a duty cycle of 0.01%. The red line represents the IV characteristics for the model while the blue line represents the measured results.

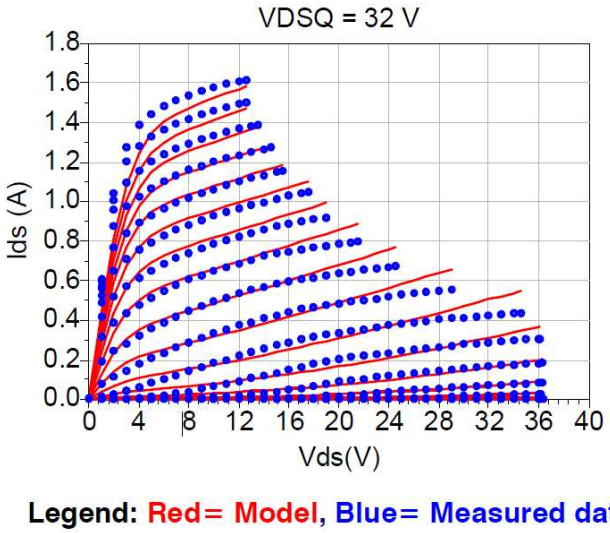


Figure 22: Ids (A) vs. Vds (V) Pulsed I-V Characteristics [20]

It can be seen in Figure 22 as I_{DS} increases, the V_{DS} must increase to produce the same quiescent current. By inspection of the IV characteristics displayed in Figure 23 we estimate a Vgs of -2.6 V is required to produce an idle quiescent current of 50 mA with a 32V V_{DD}. Please observe that as the V_{GS} gets closer to zero the quiescent current increases exponentially.

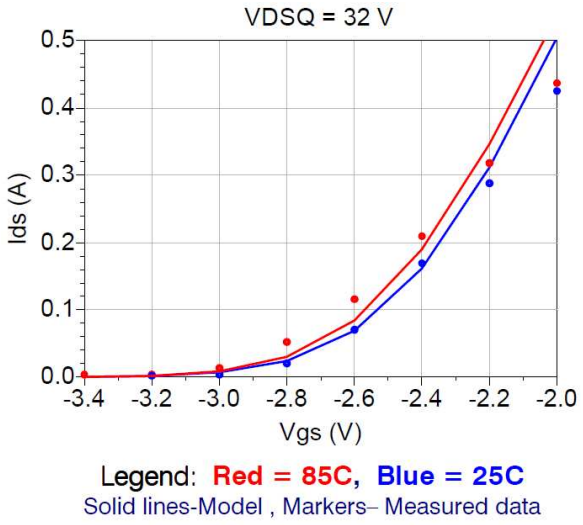


Figure 23: Ids (A) vs. Vgs (V) Pulsed I-V Characteristics [20]

The S-parameters corresponding to the pulsed I-V characteristics of VDSQ equal to 32V and IDSQ equal to 50mA are shown in Figure 24. The frequency was swept from 100MHz to 6GHz on a Vector Network Analyzer (VNA). Similarly the models response is shown in red, while the measured response is shown in blue. The S_{11} and S_{12} response produces very accurate results between the model and the measured results published by the vendor. The forward gain response for S_{21} is shown by the log mag plot and shows a distinguishable delta at lower frequencies, but should be negligible for our design frequency of 3.6 GHz [20].

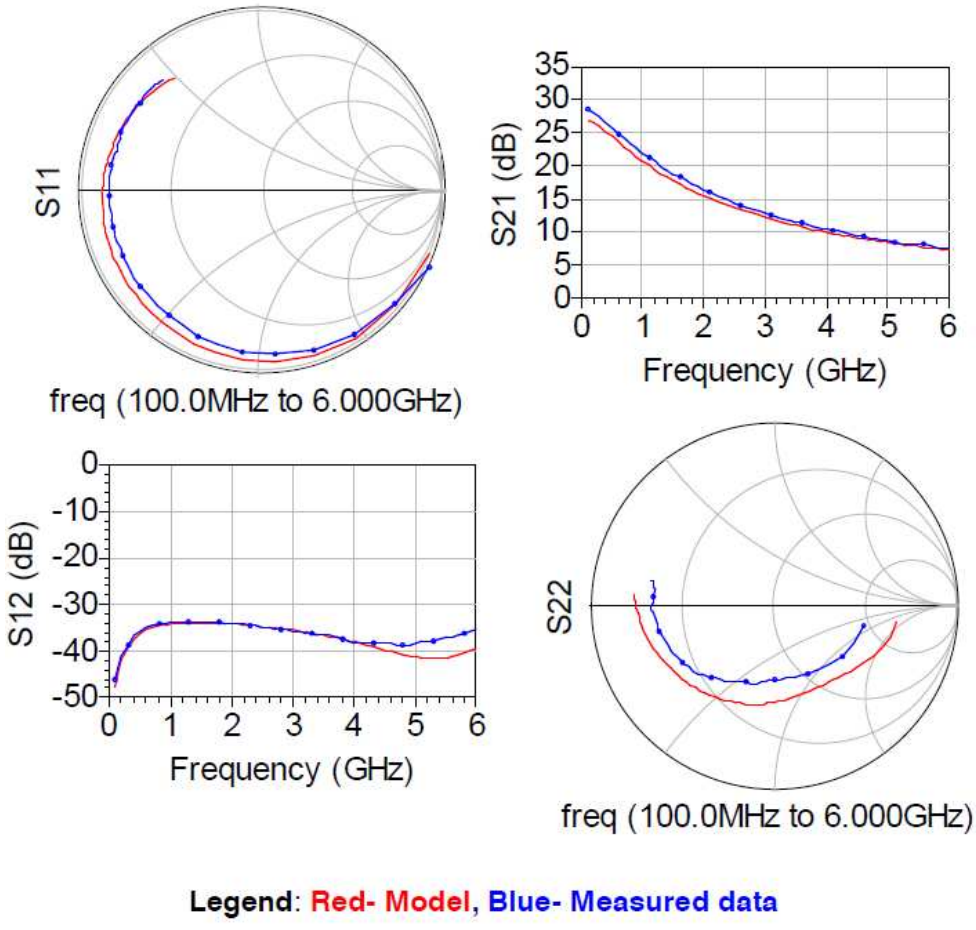
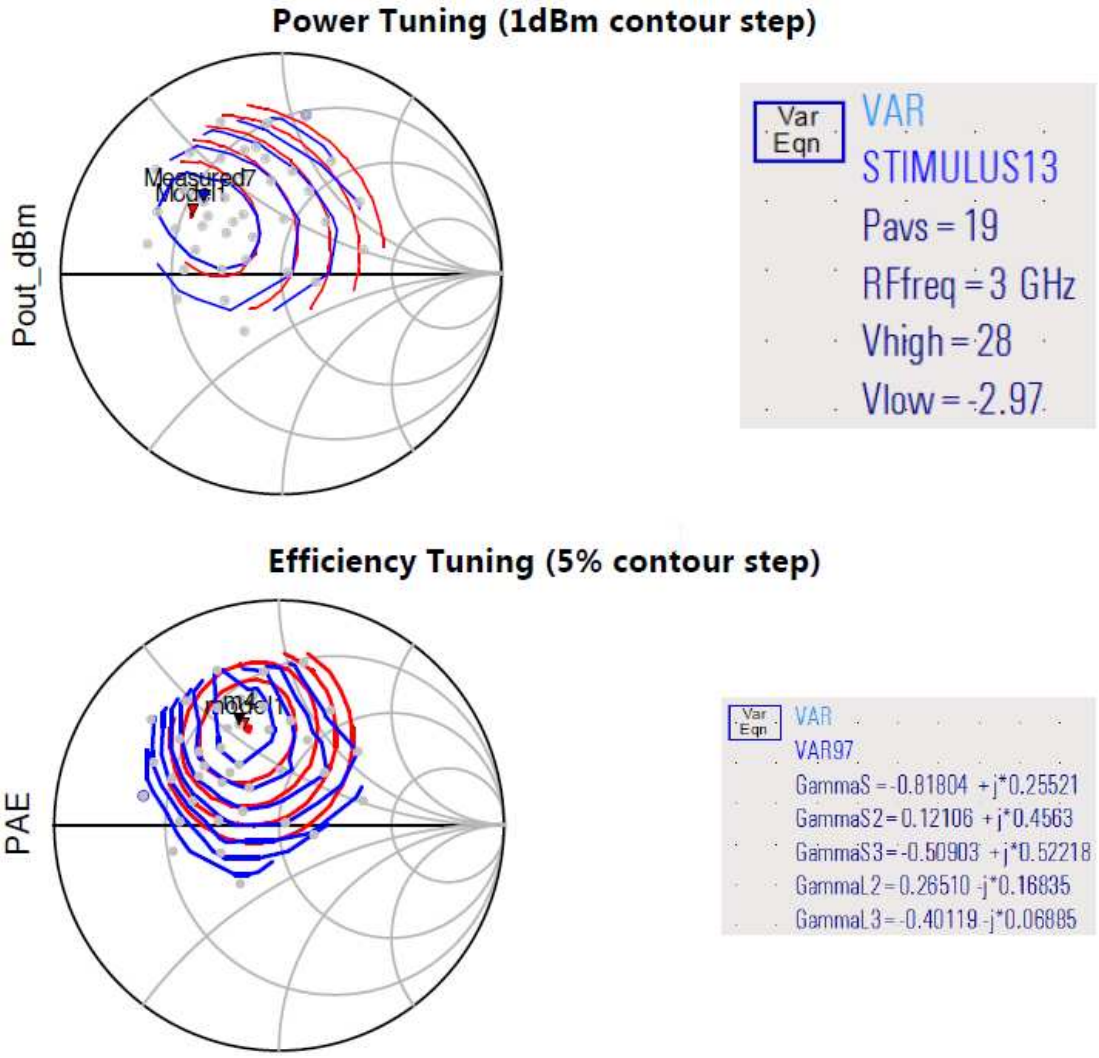


Figure 24: S-Parameter response for VDSQ = 32V and IDSQ = 50mA [20]



F = 3GHz, VDSQ = 32V, IDSQ = 50 mA, and Pin = 19dBm

Figure 25: Modelithics Load Pull Validation [20]

Table 4: Summary of Load Pull [20]

Load Pull Summary	Max Pout Load Impedance Zo*(mag/phase)	Max Pout Value (dBm)	Max PAE Load Impedance Zo*(mag/phase)	Max PAE Value (%)
Measured	Zo*(0.519/39.763)	40.2	Zo*(0.746/49.348)	76.5
Model	Zo*(0.459/33.724)	40.4	(Z0*(0.769/46.949)	72

Chapter 4
Design Process and Methodology

4.1 Design Overview

The symmetrical Doherty power amplifier is designed for high linearity using TriQuint's T1G6001032-SM GaN on SiC HEMT device with a targeted design frequency of 3.6 GHz and saturated power of 40dBm. This section describes the design process and methodology, providing a thorough discussion of the device selection, biasing circuit, matching network, combining networks, and design layout. This section will also provide relevant design simulations used to analyze each stage of the design and report the simulated figures of merit pertaining to the design of the Doherty power amplifier. The functional block diagram of the Doherty power amplifier is shown again in Figure 26.

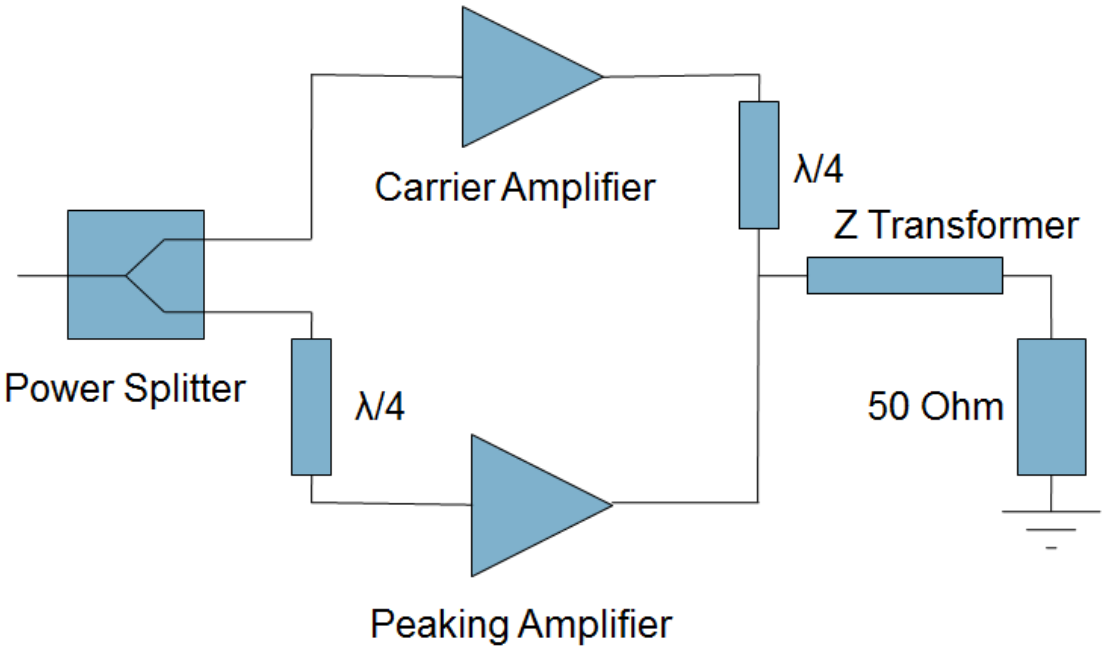


Figure 26: Functional Block Diagram of Doherty PA [7]

4.2 Device Selection

The selection of the passive circuit elements are discussed for the bias circuitry, combining network, and RF signal path and briefly covers the selection of the substrate material used for the design layout. Since the active device was described thoroughly in chapter 3, the reader is asked to refer to the previous chapter for details pertaining to the T1G6001032-SM GaN device. Table 5 list the passive component bill of materials used for the Doherty power amplifier.

Table 5: Passive Elements Bill of Materials

Reference	Value	Description	Manufacture
R1	50 ohm,	50 ohm, 10W terminator, 60120	Anaren
C1, C2, C3, C4, C9, C10, C11, C12	10pF	Cap, 10pF, 1%	AVX – ACPU
R2, R3	10 ohm	RES, 10 ohm, 1% , 1/8W, 0603	Rohm
C5, C6, C15, C16, C21, C22	10uF	Cap , 10UF , 50V, X7R, 2220	TDK
C7, C8, C13, C14	1000pF	Cap, 1000pF, X7R 1206	Murata
C17, C23	50uF 50V	Electrolytic Cap, 50uF, 50V	
C19, C20	0.2pF	Cap, 0.2pF, +/-0.1pF	ATC 600S
C21	0.8pF	Cap, 0.8pF, +/-0.1pF	ATC 600S
Splitter		3.0-4 GHz Hybrid coupler	Anaren
Connector x 2	50 ohm connector	50 ohm N type connector	Huber + Suhner
PCB		MTL D51030 2613	MTL
Base plate			RJR

The dielectric substrate selected for the 3.6 GHz Doherty power amplifier is 15mil Taconic RF35A2 and was selected based on its low losses and performance at microwave frequencies. This substrate is designed with an ultra-low fiber glass content to achieve “best in class” insertion loss properties and a homogeneous dielectric constant throughout the laminate. The uniform dispersion ceramic throughout the laminate yields extremely low coefficients of thermal expansion. The laminate is manufactured in a multi-step process that provides excellent dielectric properties as well as copper peel adhesion [21]. The dissipation factor versus frequency is shown in Figure 27. It shows a low 0.0012 dissipation factor at 3.6 GHz allowing for maximum power transfer and resulting in low heat generation. Comparing the vender’s quoted dissipation factor to Rogers 4350B laminate this is a 3x improvement, making it an ideal laminate for power amplifier applications [22].

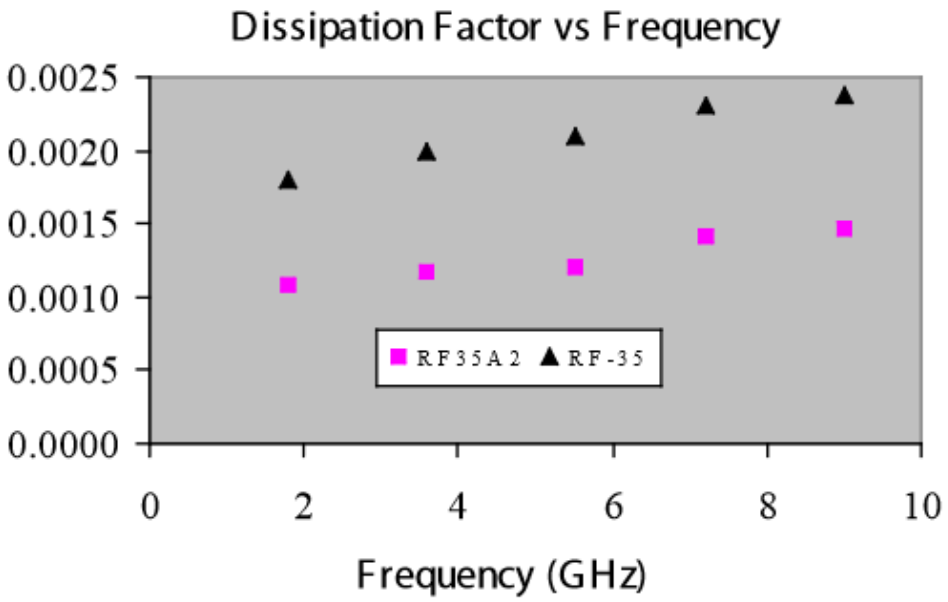


Figure 27: Taconic RF-35A2 Dissipation Factor [21]

The coupling and de-coupling capacitors selected for this design are AVX ACCU-P thin-film chip capacitors. The use of low loss dielectric materials, silicon-dioxide and silicon oxynitride, in conjunction with highly conductive electrodes results in low equivalent series resistance (ESR) and high Q. The capacitor structure for the AVX ACCU-P is shown Figure 28. These high-frequency characteristics change at a slower rate with increasing frequency than microwave ceramic chip capacitors [23]. The 0603 capacitors selected for this design has a specified tolerance of +/-1% measured at 1 MHz, and have a breakdown voltage of 50 Volts. An ESR of 132 m-Ohms at 3.6 GHz was linearly extrapolated from the data sheet which was specified at 0.9 and 2.4 GHz.

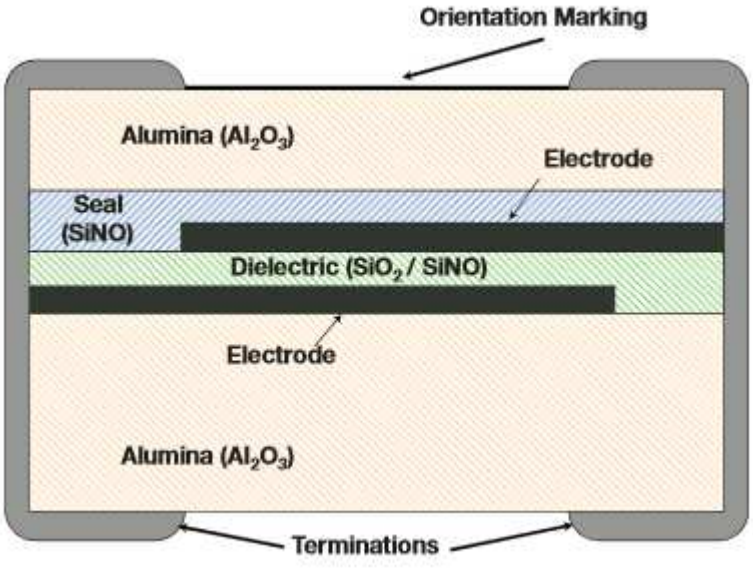


Figure 28: AVX ACCU-P Capacitor Structure [23]

4.3 Biasing Circuitry

The DC bias circuitry of the Doherty power amplifier can be divided into four individual circuits designed to deliver the required drain and gate voltages to the carrier and peaking amplifier. To isolate the RF from the DC power supply a quarter-wavelength transmission line is used as an RF choke so that DC appears as a short-circuit at the gate and drain while at microwave frequencies it appears as an open-circuit. Several shunt capacitors are used absorb current spikes caused from supply ripple while also decoupling any RF from the DC power supply. A series resistor is used at the input of the gate to further absorb noise from the power supply or RF leaking into the power supply. The bias circuitry for the carrier and peaking amplifiers are identical and is represented by the circuit model shown in Figure 29.

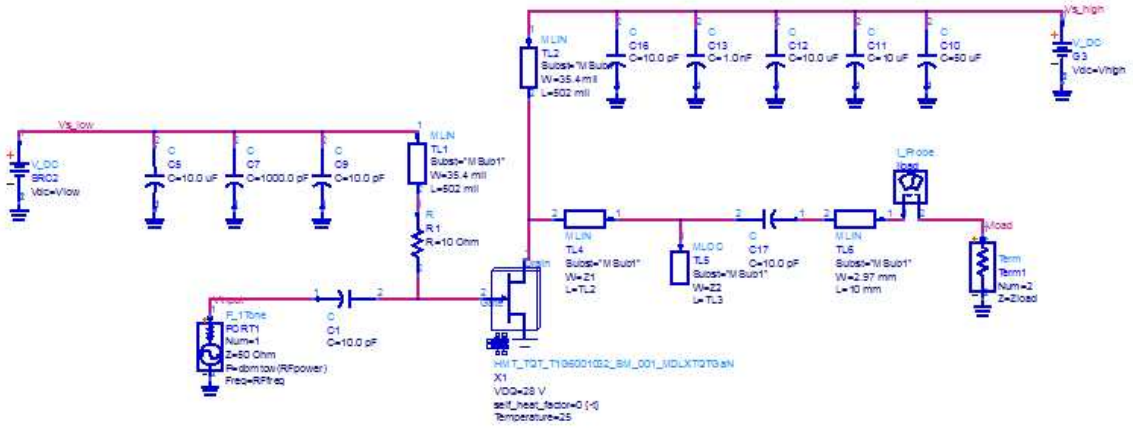


Figure 29: Circuit model of the bias circuitry

A microstrip line is a transmission line consisting of a strip conductor and a ground plane separated by a dielectric medium [14]. To determine the length of our quarter-wavelength transmission line we must first determine the phase velocity, $v_{p,}$ given by the following equation.

$$v_p = \frac{c}{\sqrt{\varepsilon_{ff}}} \tag{4.1}$$

Where c is the speed of light (3 x 10^8 m/s) and ε_{ff} is the effective relative dielectric constant of the dielectric substrate. We can determine the effective relative dielectric constant of the 15 mil RF35A2 Taconic substrate by using the following equation.

$$\varepsilon_{ff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left[\frac{1}{\sqrt{1 + 12 \cdot H / W}}\right] \tag{4.2}$$

Where ε_r is the dielectric constant of the substrate, H is the height of the substrate, and W is the line width of the microstrip. Inserting the properties of the Taconic RF35A2 substrate into the equation 4.2 returns an ε_{ff} equal to 2.658. We can then determine the line length of the quarter-wavelength transformer from the following equation.

$$l = \frac{90^o \left(\pi / 180^o\right)}{\sqrt{\varepsilon_{ff}} \cdot k_o} \tag{4.3}$$

Where k_o is equal to the inverse of the wavelength in free space, given by the following equation.

$$k_0 = \frac{2\pi f}{c} \tag{4.4}$$

Finally, we can determine that the length of the quarter-wavelength in the 15 mil RF35A2 Taconic substrate is approximately 1.29 cm or 502 mil. This value will be used to approximate the placing of the 10 pF decoupling capacitor and will be referenced for the quarter-wavelength transformer in the output combining network of the carrier amplifier.

4.4 Input Combining Network

The symmetrical Doherty PA design requires that the RF input power to be equally split between the carrier and peaking amplifier. This is more commonly performed using a Wilkinson power divider which can be realized with microstrip and a chip isolation resistor. However, since the peaking amplifier requires a 90 degree phase delay at its input, it is advantageous to employ a 90 degree 3dB hybrid coupler to accomplish the power splitting and phase delay functions.

The 90 degree hybrid coupler selected for this design is an Anaren XC3500P-03S high performance 3dB hybrid coupler intended for use between 3.3 GHz and 3.8 GHz. It is packaged in a low-profile manufacturing-friendly surface mount package. It is designed particularly for balanced power and low noise amplifiers, plus signal distribution and other applications where low

insertion loss and tight amplitude and phase balance is required. It can be employed in power applications up to 55 Watts, which is more than enough power handling capabilities for the 10 Watt Doherty power amplifier design [24].

The electrical specifications call out a minimum isolation of 21dB, a maximum insertion loss of 0.25dB, a maximum VSWR of 1.20, and a maximum amplitude balance of +/- 0.25 dB. The phase delay is specified with a tolerance of +/- 3 degrees and must be accounted for later in the design process. This device can be operated over a wide temperature from -55℃ to +85℃. The 90 degree hybrid coupler pin configuration can be seen in Figure 30. Since this device can be used in combiner and splitter applications, the pin out configuration can be used so that the device is oriented 90 degrees counter clockwise such that pin 1 is the isolation port, pin 2 is the input port, pin 3 is the -3dB port connected to the carrier amplifier, and pin 4 is –3dB with a -90 degree delay connected to the peaking amplifier.

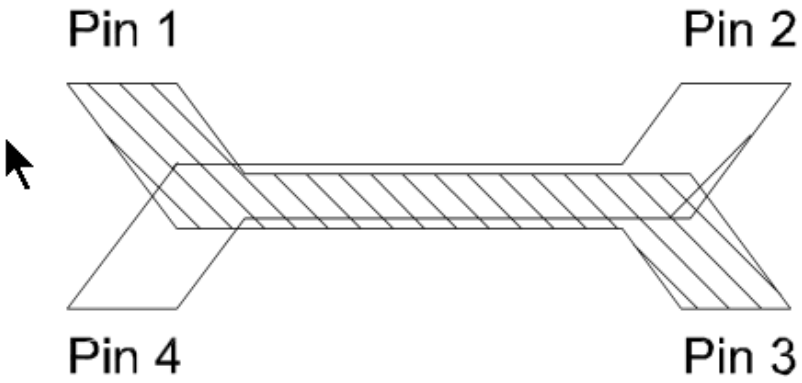


Figure 30: The XC3500P-03S 3dB Hybrid Coupler Pin Configuration [24]

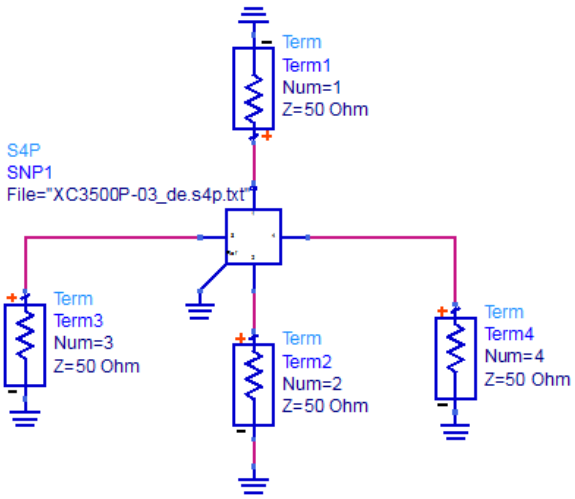


Figure 31: Data Item used to import S4P data

Using the vender supplied 4 port S4P touchstone file the performance of the 3dB 90 degree coupler was evaluated using the data item feature in ADS. Once the 4 port touchstone file was imported using the data item feature shown in Figure 31, the output performance of the device reported a magnitude imbalance on ports 3 and 4 to be approximately 0.1 dB at 3.6 GHz. The phase delta between ports 3 and 4 was approximately -90.8 degrees which meets the +/- 3 degrees specified in the device's data sheet.

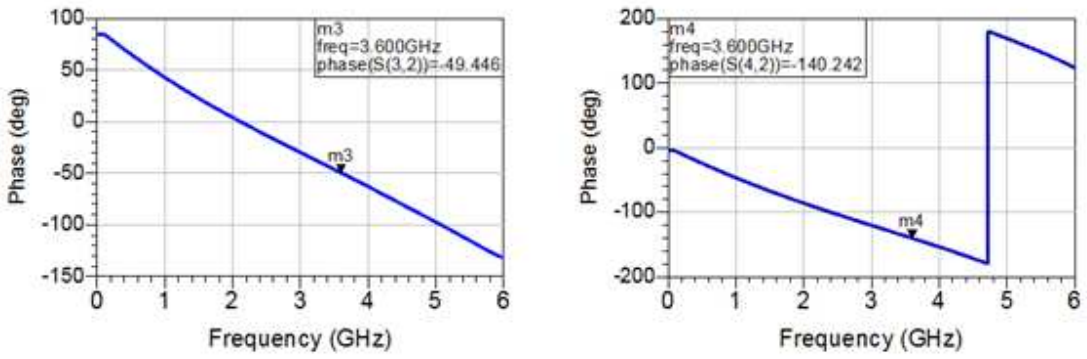


Figure 32: Output performance of 3dB Hybrid Coupler

Having found reasonable performance from the 3dB 90 degree coupler, the phase difference at the input of the carrier and peaking amplifier must be verified. This was achieved by modeling the layout of the Taconic RF35A2 substrate and the design layout leading up to the input of the carrier which can be seen in Figure 33.

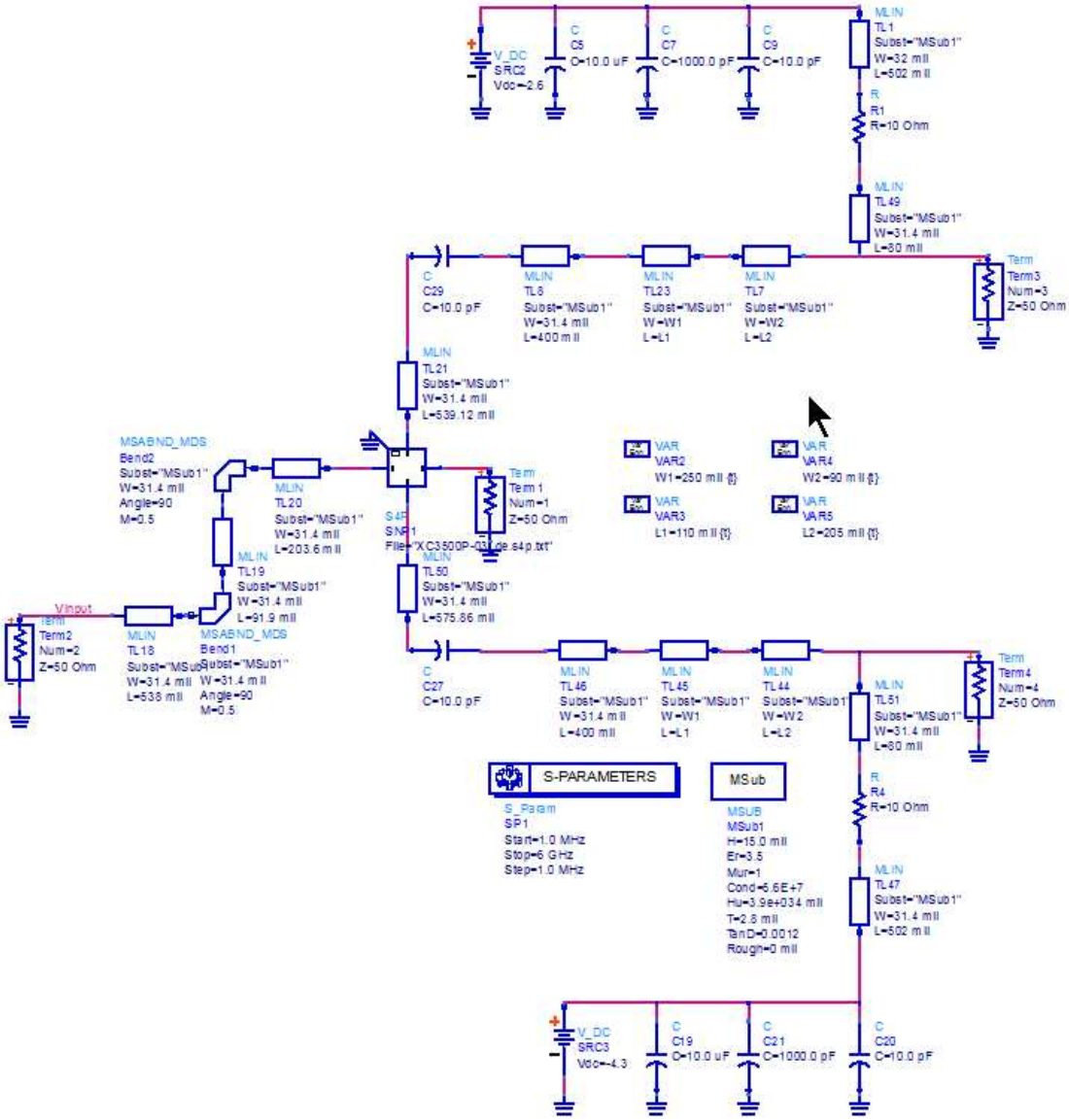


Figure 33: Circuit model to test input combining network

A small-signal S-parameter simulation in Figure 34 shows the phase delta at the input of the transistors is approximately 89° between the carrier and peaking amplifier at 3.6GHz. This meets the impedance inversion requirements of the input combining network.

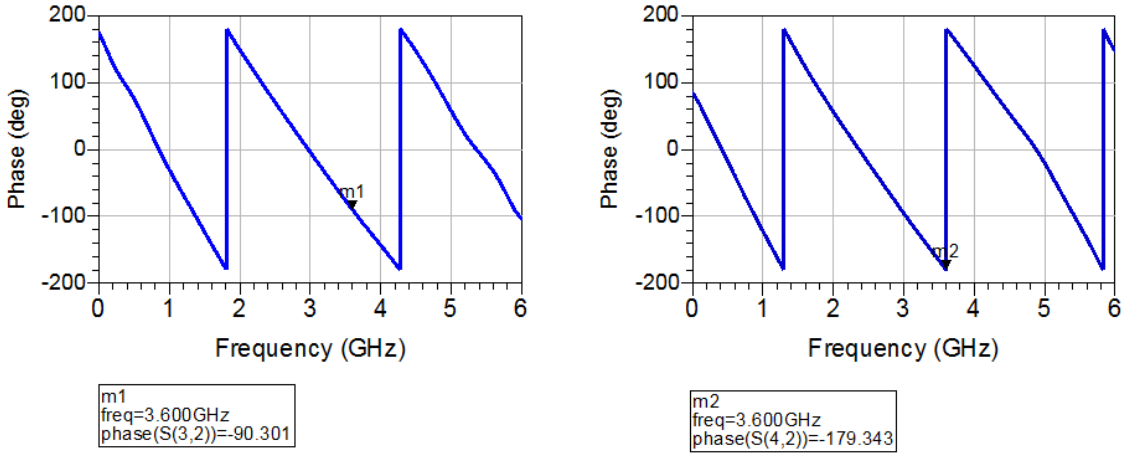


Figure 34: Simulation results of input combining network

4.5 Input and Output Matching Networks

The input and output matching network for the carrier and peaking amplifier were determined by running harmonic balance simulations in ADS and tuning the widths and lengths of the transmission lines until the maximum gain and PAE were reported. Tunable variables were deployed to find the optimal width for each segment of transmission line for the input and output matching network of the carrier and peaking amplifier which can be seen in Figure 35 below. This iterative process made design of the input and output matching networks straight forward. Starting from the left and moving to the right the variables were tuned until a relative maxima for gain and PAE were found before proceeding to the next variable.

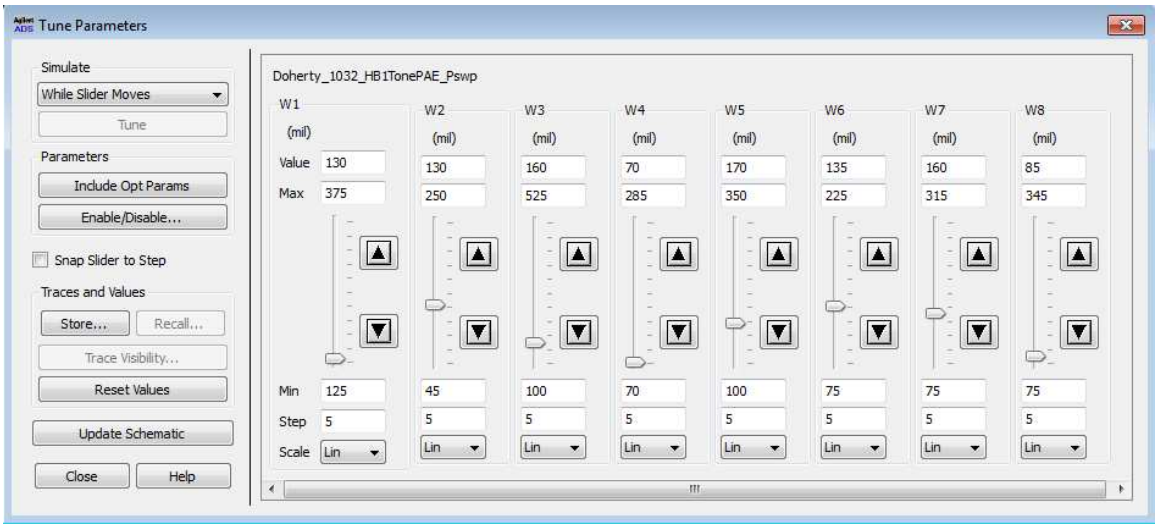


Figure 35: Matching Network Transmission Line Tuning

The classical design approach would opt for a source-pull analysis to determine the impedance looking into the transistor to return the maximum gain. Then the transmission line impedance matching network would be design to match the 50 ohm source impedance to the input impedance of the transmission line. This approach is time-consuming, tedious, and prone to calculation error given the nature of the transmission line formulas [14]. Having performed these calculations in the past, a deep appreciation for working design models alleviates this facet of the design process.

4.6 Zopt Impedance Selection

In the design of classical symmetric Doherty power amplifiers, the selection of the carrier amplifiers Zopt condition is critical to the amplifiers saturated power characteristic. Less emphasis toward the selection of the Zopt impedance is described here because a softer efficiency peak at backed-off power levels was required to meet linearity requirements, which will be discussed

momentarily. This implies that the carrier amplifier is still behaving linearly when the peaking amplifier begins to turn on. This differs from the design of the classical symmetric Doherty power amplifier which requires that the carrier amplifier is saturated before the peaking amplifier begins to turn on, resulting in a sharp efficiency peak at backed-off input power.

However, to achieve the sharp efficiency peak which is exemplary of the classical Doherty design the selection of Zopt must meet three criteria simultaneously and are discussed here to give depth and thorough treatment of the Doherty power amplifier.

1. Zopt must provide saturated power when both the carrier and peaking amplifier are fully on.
2. 2*Zopt at a 2:1 VSWR centered around Zopt delivers the best possible efficiency.
3. Zopt and off-state of the peaking amplifier must be able to achieve high impedance into the Doherty combining network.

In the classic approach of selecting the Doherty amplifiers target impedance, we must consider many factors including gain, power, and efficiency. Trade-offs will need to be made to best meet our design criteria. An ideal device would have max power and max efficiency exactly separated by a 2:1 VSWR. The power and efficiency contours would oppose each other perfectly. In reality few devices follow an ideal impedance trajectory. Therefore, to maximize the back-off efficiency it is important to look at load pull data at the target average power in addition to saturated conditions.

4.7 Output Combining Network

The output combining network of the 3.6 GHz Doherty power amplifier was designed using transmission lines. A quarter-wavelength transmission line on the output of the carrier amplifier was employed to sum the signals back together so that the phases at the recombination nodes were equal. The method for evaluating phase at this recombination node was by modeling this network shown in Figure 36.

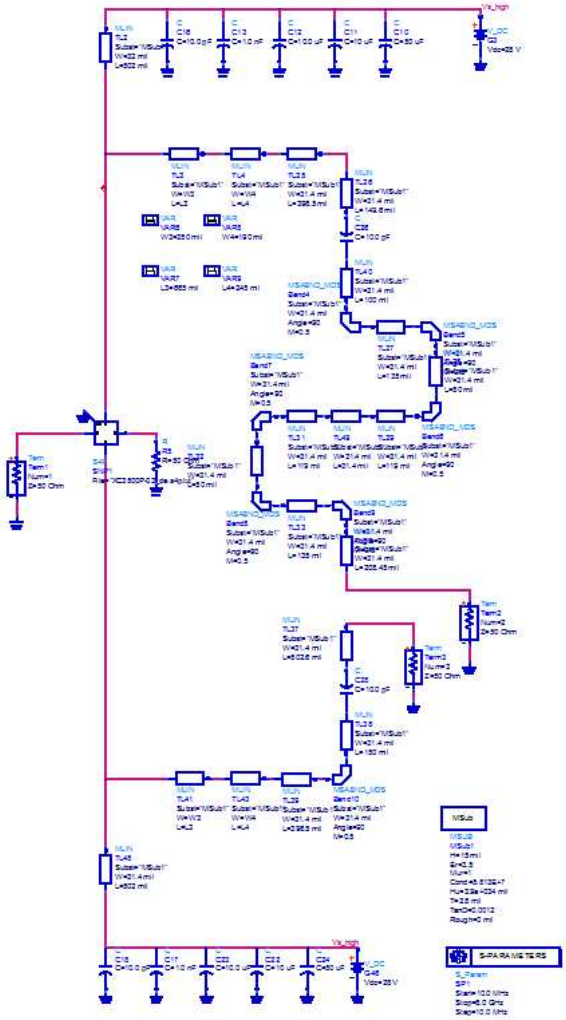


Figure 36: Output Combining Network

The transistors were replaced by the Anaren XC3500P-03S high performance 3dB hybrid coupler to produce a 90 degree output of phase response at the input of the carrier and peaking amplifiers output matching networks. At the recombination node where the output of the carrier and peaking amplifiers meet the circuit was broken and terminated with 50 ohms so that small-signal S-parameters simulations could measure the phase going into the recombination node. The simulated results shown in Figure 37 shows the phase at the recombination node are approximately equal.

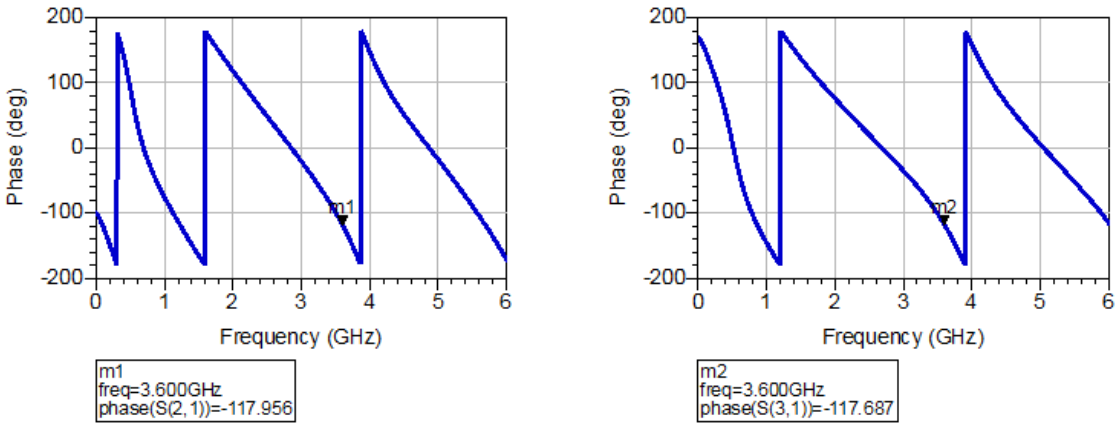


Figure 37: Simulated Phase at Recombination Node

4.8 Off-State of Peaking Amplifier

When the input-power is completely backed-off the peaking amp should be inactive and “invisible” to the carrier amplifier. In order to achieve this it is desirable to achieve an open-circuit from the combining node of the peaking-amplifier. The off-state impedance measured by the small-signal matching network, should create an open-circuit into the recombination node. A simulation

in ADS was setup to measure the off-state impedance of the peaking amplifier and its circuit model representation is given in the Figure 38 below.

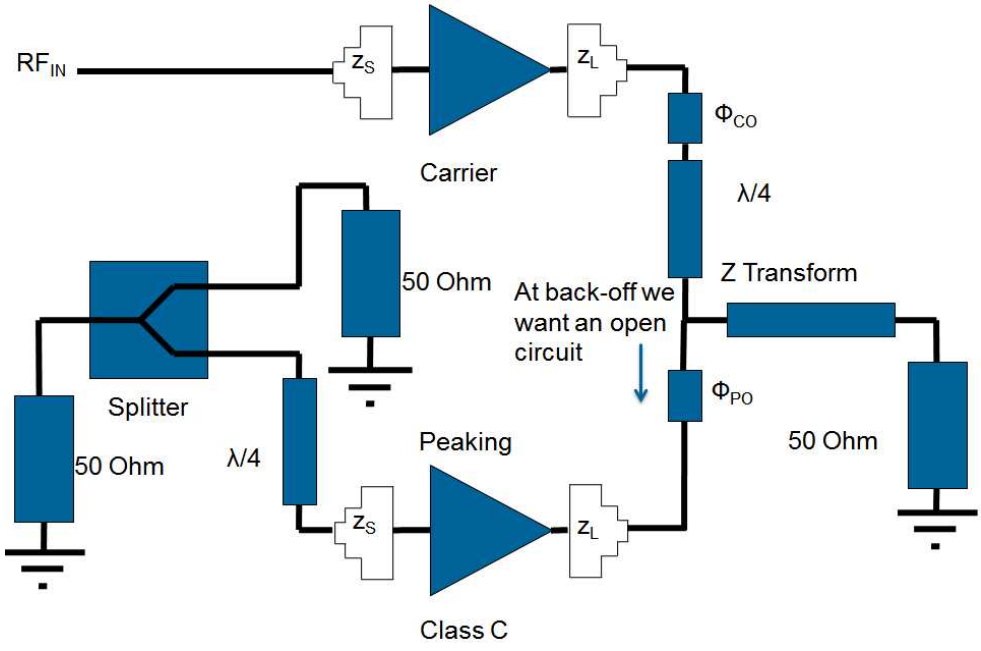


Figure 38: Circuit Model Representation to Measure Off-state Impedance [7]

The circuit was broken at the recombination node and a 25 ohm terminal was placed at the peaking amplifiers recombination node to replicate the ideal modulated impedance Z_m. The off-state impedance of the peaking amplifier was simulated using small-signal S-parameters and the transmission line length depicted by $\square_{PO}$ was tuned to optimize the highest attainable impedance into the peaking amplifiers recombination node. Moreover, to confirm that the peaking amplifier was in its off-state due to the implications of Class-C biasing, the amplifier was connected in Doherty mode and the same high-Z impedance was measured at the recombination node of the peaking amplifier confirming the off-state of the peaking amplifier. This normalized off-state impedance is shown below in Figure 39 and corresponds to a real impedance of 365 ohms.

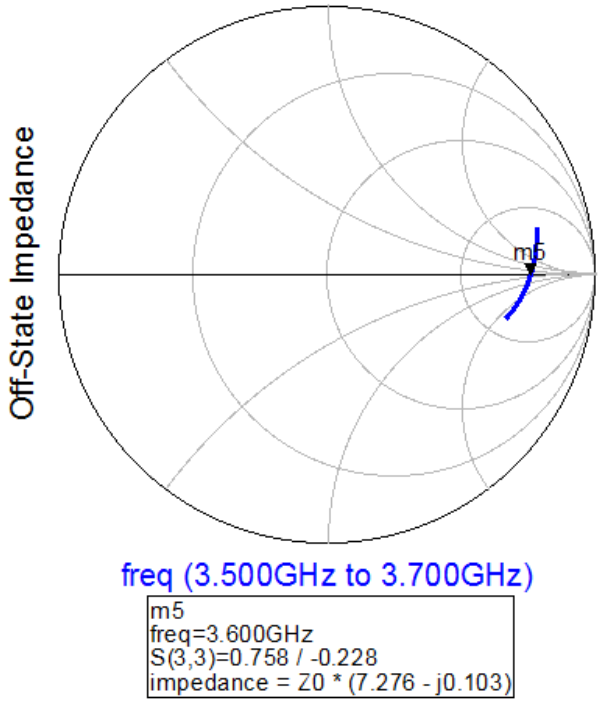


Figure 39: Simulated Off-State Impedance of Peaking Amplifier

4.9 Output Impedance Transformer

The output impedance transformer for the Doherty power amplifier was created using a microstrip quarter-wavelength transformer. From the recombination node the modulated impedance is approximately half that of the 50 ohm system impedance. Therefore, an output transformer is required to convert the 25 ohm modulated impedance to the 50 ohm system impedance. A quarter-wavelength transformer is employed to convert the modulated impedance to the system impedance, ensuring the maximum power transfer to the load is being satisfied. The calculation to determine the impedance of the output transformers transmission line is shown.

$$Z_T = \sqrt{50\Omega \cdot 25\Omega} = 35.4\Omega \quad (4.5)$$

Referring to equations 4.1 through 4.4 we calculated the length and width of the microstrip quarter-wavelength transformer and determined that the length to be 489 mils and the width to be 51.4 mils.

4.10 Final Design

The final design of the 3.6 GHz Doherty power amplifier was simulated using ADS to model the 15 mil Taconic RF35A2 substrate, PCB design layout, passive, and active models. The final design was evaluated by its small signal S-parameters, large-signal single-tone PAE and gain, two-tone PAE, gain and carrier to IMD ratio. The most critical of these parameters being the carrier to intermodulation distortion ratio reported during the two-tone PAE vs swept input power simulations. To achieve a carrier to IMD ratio greater than 30 dB, while maximizing PAE, the transmission line dimensions of the input and output matching networks were tuned. This resulted in a design tradeoff between its maximum PAE and backed-off PAE in exchange for improved linearity. The final circuit model used to evaluate the 3.6 GHz Doherty power amplifier can be seen in Figure 40.

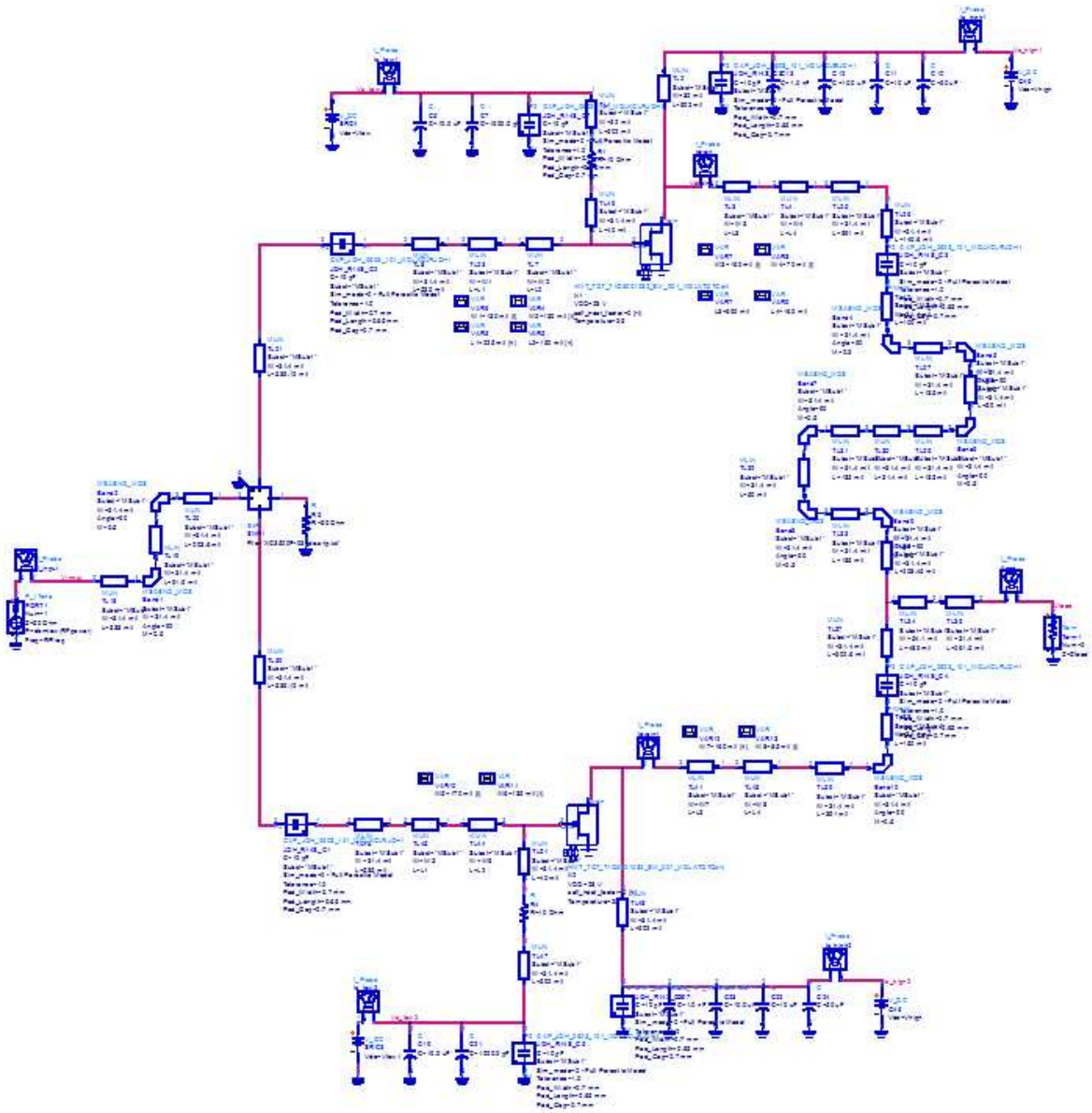


Figure 40: Circuit Model of 3.6 GHz Doherty Power Amplifier

4.11 Simulated Results

This section will reports the simulated results of the final design shown in Figure 38. The first of which are the small-signal S-parameters swept from 100 MHz to 6 GHz shown in Figure 41. It should be mentioned that the frequency

response is a result of the carrier amplifier because the peaking amplifier is in an "off-state" for small-signal analysis due to the Class-C biasing.

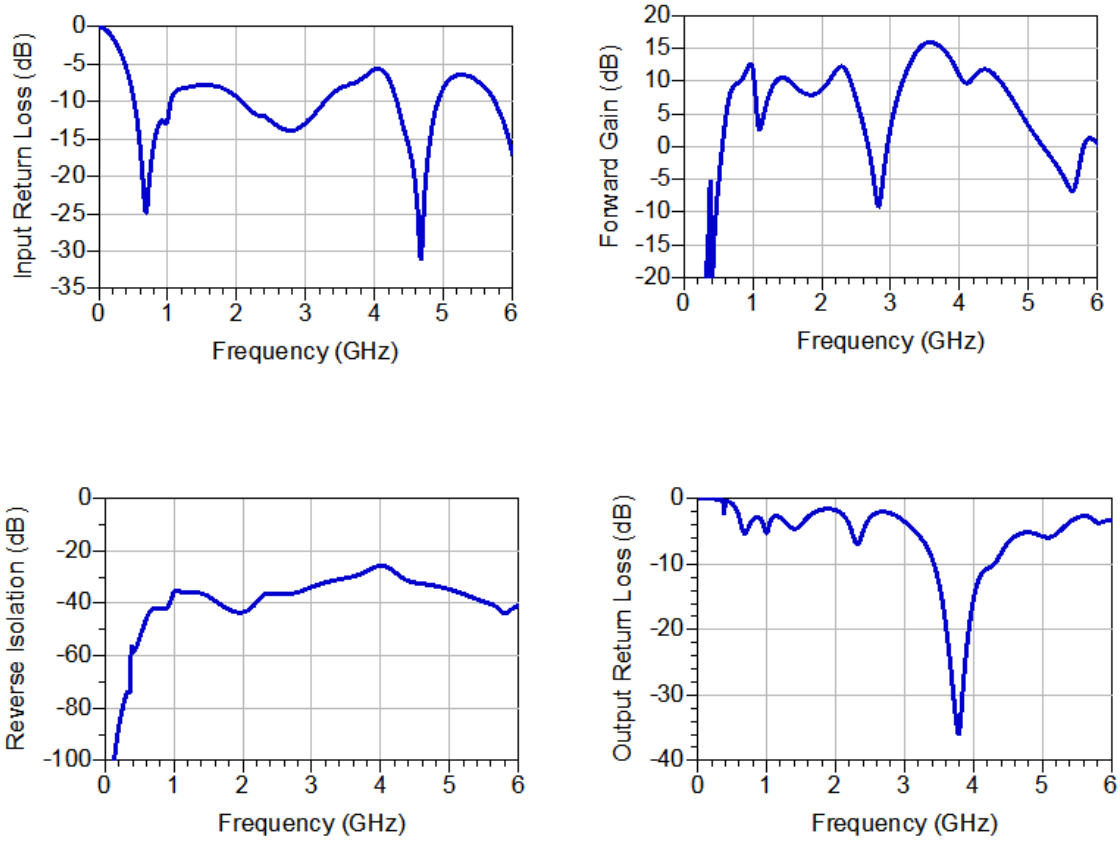


Figure 41: Simulated Small-Signal S-parameters

The single-tone harmonic balance simulation was used to sweep the input power from 10 dBm to 27 dBm in 1 dB increments. The result show the transducer power gain (dB) and PAE(%) in Figure 40 below. The simulated transducer power gain is approximately 15.5 dB until it approaches approximately 34 dBm and a pronounced dip in gain can be observed. This dip in gain is due to the interaction between the carrier and peaking amplifier. This is the instantaneous power where the peaking amplifier is beginning to contribute to the output of the Doherty power amplifier.

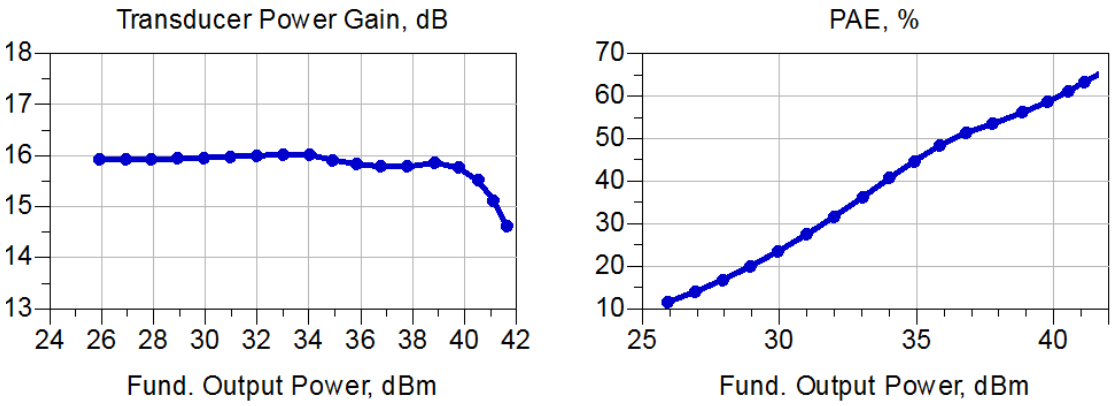


Figure 42: Simulated transducer power gain and PAE

The simulated single-tone large signal PAE shown in Figure 42 reported a maximum 64.5%, and a PAE of 50.4% when the input power is backed-off by 6 dB. The soft efficiency peak is evident and is an indicator that the carrier amplifier is still operating linearly as the peaking amplifier begins to contribute to the RF output power.

A two-tone harmonic balance simulation was used to record the two-tone IMD measurements reported in Figure 43. The transducer power gain, PAE, 3rd-Order, and 5th-Order IMD products are shown. Please observe that the carrier to intermodulation ratio no longer meets the 30 dBc specification at approximately 35 dBm.

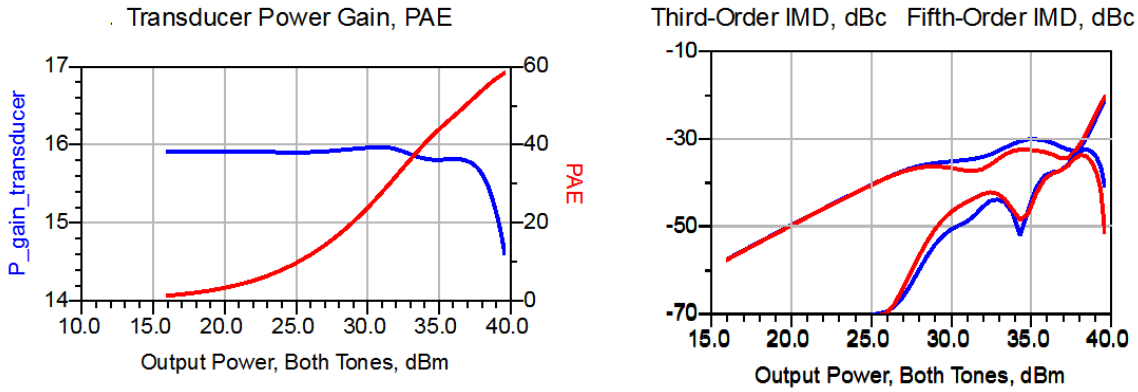


Figure 43: Simulated Two-Tone Gain, PAE, 3rd-Order IMD, 5th-Order IMD

4.12 Layout

The design layout 3.6 GHz Doherty power amplifier was created using the layout feature in ADS and can be seen in Figure 44. The PCB design layout is designed so that it can be mounted to an existing 4” x 4” aluminum base plate used to dissipate the heat created by the device. This layout features adequate grounding with numerous vias connecting the top metal to the ground plane.

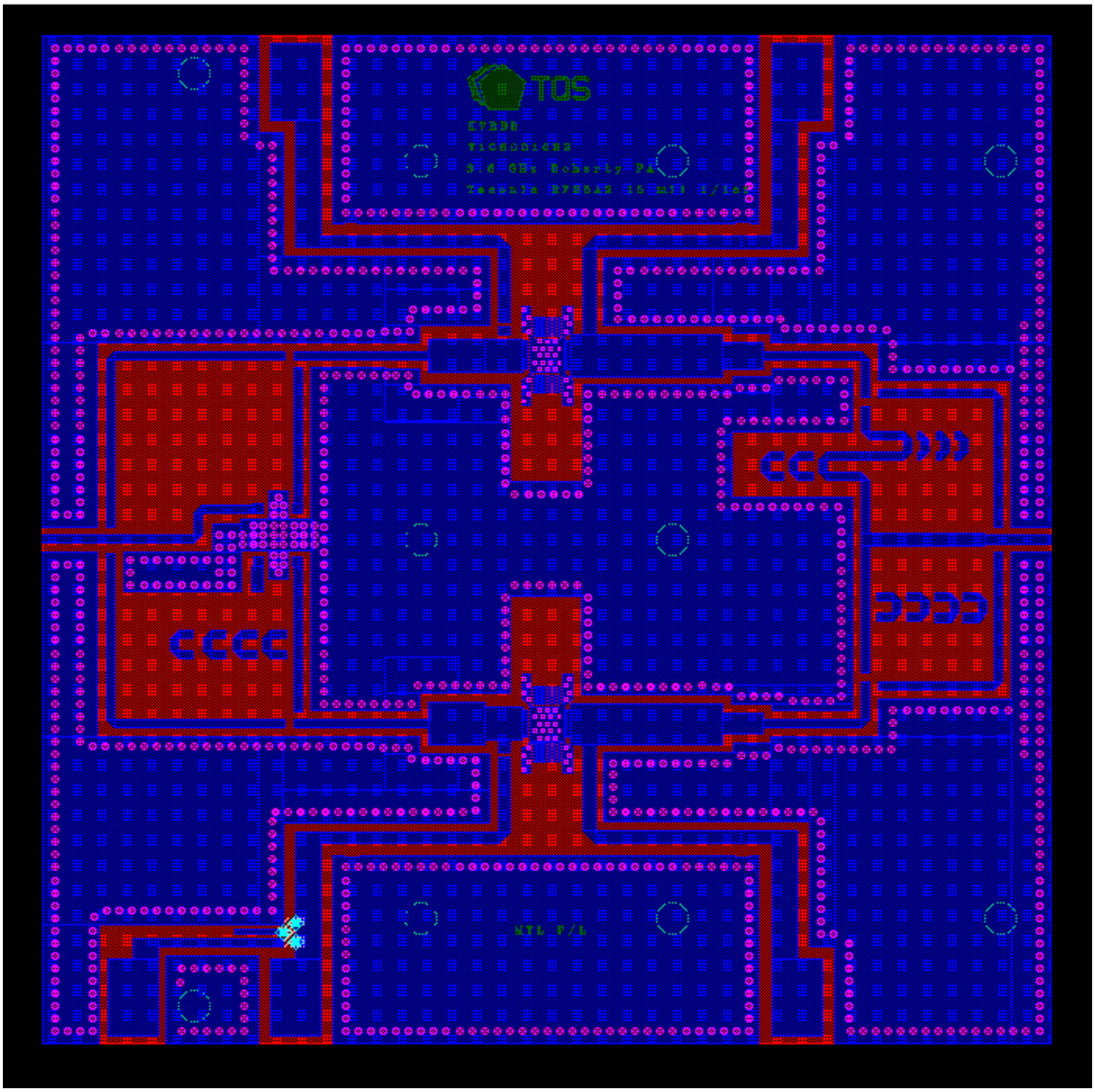


Figure 44: Design layout of 3.6 GHz Doherty Power Amplifier

RF paths for the carrier and peaking amplifier are included to tune and evaluate and the performance of each amplifier. Tuning handles are included to the carrier and peaking amplifiers output combining networks as well as the peaking amplifiers input combining network. This feature is used to tune the input and output combining network to achieve the desired phase performance for their respective networks.

Should the user be constrained by the use of two individual power supplies, the layout also includes an optional voltage regulator on the gate supply of the peaking amplifier. This would enable the user to add a low-drop out (LDO) negative voltage regulator such as the Maxim 1735 which comes in a 5 pin, SOT-23 package. This device operates from -2.5 to -6.5 Volts input voltage and can supply an output from -1.25 to -5.5 Volts with the use of an external voltage divider. This device guarantees a 200 mA maximum output current with a low voltage dropout of 80mV. The guaranteed maximum output current of 200 mA is more than sufficient to supply the near zero gate current of the T1G6001032-SM GaN HEMT device and the 80mV low-voltage dropout is more than enough to supply the -2.6 to -2.8 Volts needed for the gate of the carrier amplifier from the -4.3V pinched off gate voltage of the peaking amplifier.

4.13 Assembly Method

The assembly of the 3.6 GHz Doherty power amplifier begins by soldering the PCB to the 4” x 4” aluminum heat sink with nickel-tin plating, making it possible to solder the heat sink to the back metal of the PCB. A hotplate and lead based solder was required to mount the test fixture to the aluminum base

plate. We found through trial and error that applying a thin coat of lead based solder to the baseplate produced the best results. The Taconic RF35A2 test fixture is then mounted to the base plate and mounting screws are used to hold the test fixture in place during the solder flow process. A temperature of 280° C is used to flow the solder between the nickel-tin plated aluminum heat sink to the back metal of the Taconic RF35A2 substrate. Once the test fixture has cooled it is placed in an ultrasonic alcohol solution to clean any excess flux that accumulated during the solder flow process.

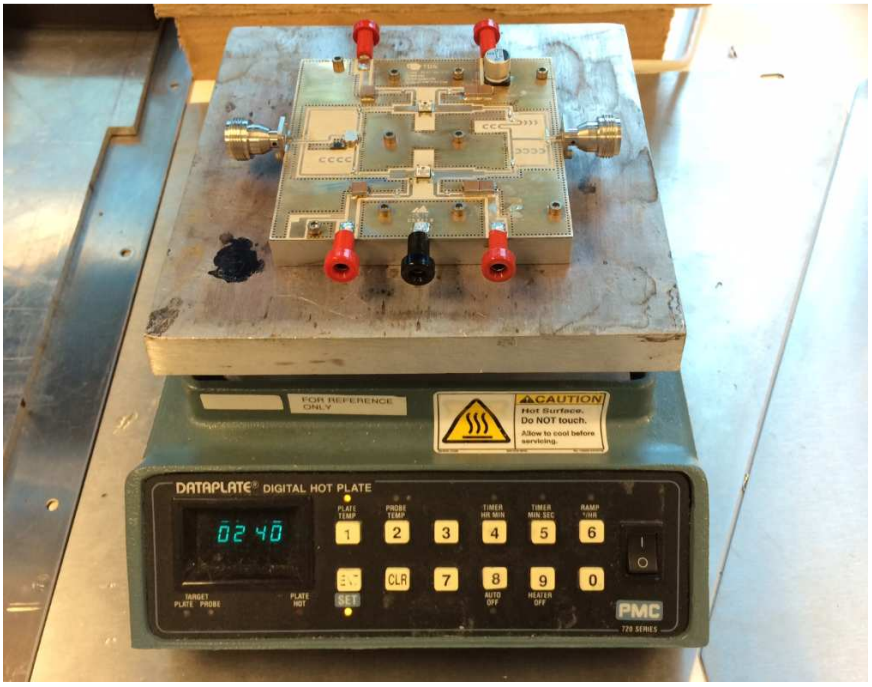


Figure 45: Hot Plate Assembly of SMD Components

Once the test fixture has been cleaned the passive and active components can be mounted to the test fixture. This is achieved by setting the temperature of the hotplate to 240℃, allowing solder to flow between the top metal of the PCB and surface mount components, shown in Figure 43. This step

would be repeated several times during the tuning of the Doherty power amplifier. It was necessary to test the carrier and peaking amplifiers individually to ensure adequate performance. Female banana plugs with flat metal leads were soldered to the top metal of the PCB using a more traditional soldering iron making it easy to connect DC power to the test fixture. Finally the assembled test fixture is connected in Doherty mode which can be seen in the Figure 46.

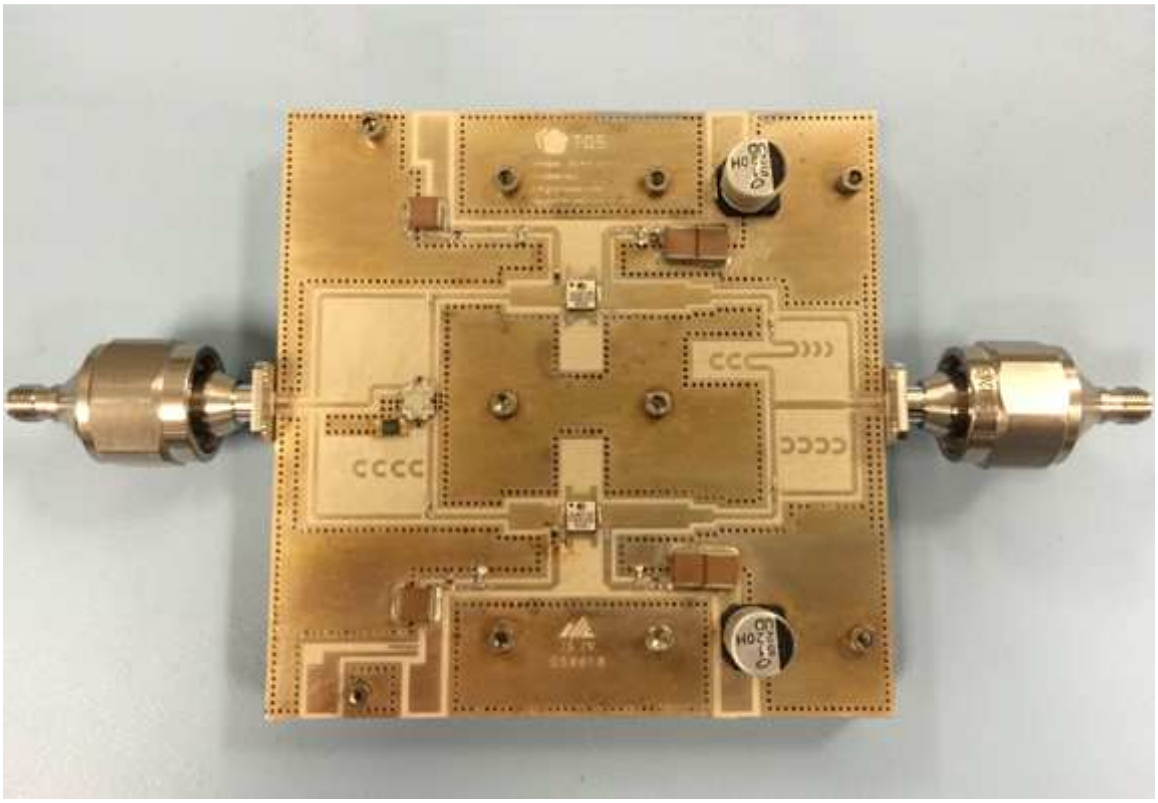


Figure 46: Assembled 3.6 GHz Doherty Power Amplifier

Chapter 5
Power Amplifier Measurements

5.1 Test Instruments

The 3.6 GHz Doherty power amplifier was tested on the bench and its performance was evaluated against the simulated performance first presented in the previous chapter. The precision instruments used to test the device under test (DUT) are listed in table 6. Four DC power supplies were used to power the individual gates and drains of the power amplifier. A pair of Agilent E4438C ESG were used for two-tone IMD measurements in conjunction with a MiniCirucits 3dB splitter. A single ESG was used for single-tone tests. Due to the output power limitations of the Agilent E4438Cs an Amplifier Research (AR) 5S1G4M2 800 MHz to 4.2 GHz power amplifier was used to adequately drive the Doherty power amplfier into saturation.

Table 6: Test Equipment

Make	Model	Quantity	Description
Agilent	E3631A	2	DC Power Supply
Agilent	E3662A	2	DC Power Supply
Agilent	E4438C	2	ESG 250 kHz to 4 GHz
Agilent	ENA E5071B	1	Vector Network Analyzer
Agilent	E4418B	1	Power Meter
Agilent	E9300A	1	Power Sensor
AR	5S1G4M2	1	800 MHz to 4.2 GHz Power Amp
R&S	FSV	1	Signal Analyzer 9 kHz – 30 GHz
Narda	4226-20	1	20 dB Directional Coupler
MiniCircuits	ZFSC-2-10G	1	Power Splitter
Meca	IS-3000	1	Isolator 3 GHz – 4.8 GHz

From the output of the AR amplifier a 24” piece of coax is used which terminates to a Meca isolator to ensure that energy flows in one direction. This is an extremely useful device for isolating components in a chain, to prevent any voltage standing wave ratio (VSWR) at the input of the DUT. From the output of the DUT the RF signal goes into a Narda 20 dB directional coupler, so that the signal coming out of the coupled port is attenuated by 20 dB before it is received on the R&S FSV signal analyzer. This is a necessary precaution since the instruments receiver can be damaged by RF signals greater than 30 dBm. The output of the directional coupler is also padded with a 20 dB attenuator to prevent damaging the power sensor of the Agilent E4418B power meter

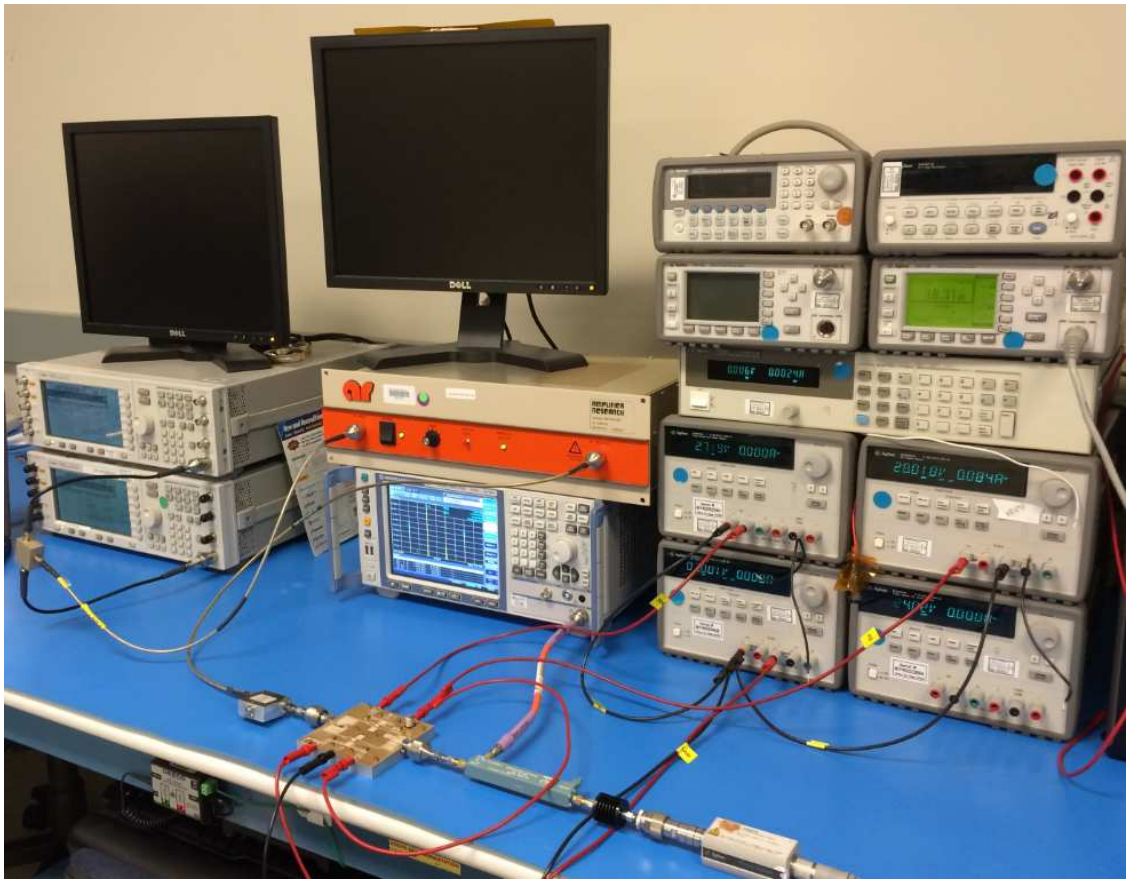


Figure 47: Two-Tone IMD Large-Signal Bench

5.2 DC Biasing

The Doherty power amplifier was DC biased to produce a quiescent current of 100 mA by setting Vgc to 2.7 V and a Vdd of 28 V, where the gate voltage on the peaking amplifier is pinched off to -4.3 V to achieve a Class-B bias. The turn-on and shut-down sequence of the power supplies is absolutely critical to avoid damaging the T1G6001032-SM GaN devices. Since these devices are biased in depletion mode applying a more negative voltage on the gate pinches off the channel. If the Vdd is turned on with 0 Volts on the gate, the channel is wide open and current will be near Idss. The turn-on and shut-down sequence should be followed at all times. Not following this protocol **will** damage the device resulting in gate leakage currents.

Turn-on	**Shut-down**
1. Vgc	1. RF
2. Vgp	2. Vdd
3. Vdd	3. Vgp
4. RF	4. Vgc

To eliminate any voltage drop across the DC cables, custom 16 gauge cables were created for the carrier and peaking amplifier drain supplies that terminated the force and sense lines at the DC input of the DUT. The use of individual DC power supplies allowed us to accurately monitor the currents being sourced from each of the individual supplies, and more importantly shows the instantaneous power at which the peaking amplifier turns on.

5.3 Small-Signal Testing

The small-signal scattering parameters were measured using an Agilent ENA E5071B. The instrument was calibrated using its accompanying E-cal and setup for a broadband sweep from 1 MHz to 6 GHz with a -30 dBm source signal. The simulated (blue) and measured (red) results are shown in Figure 48 shows that the simulated and measured results line up reasonably well. The small-signal S-parameters are due solely to the carrier amplifier because the instantaneous power level of the power amplifier is not large enough to activate the peaking amplifier.

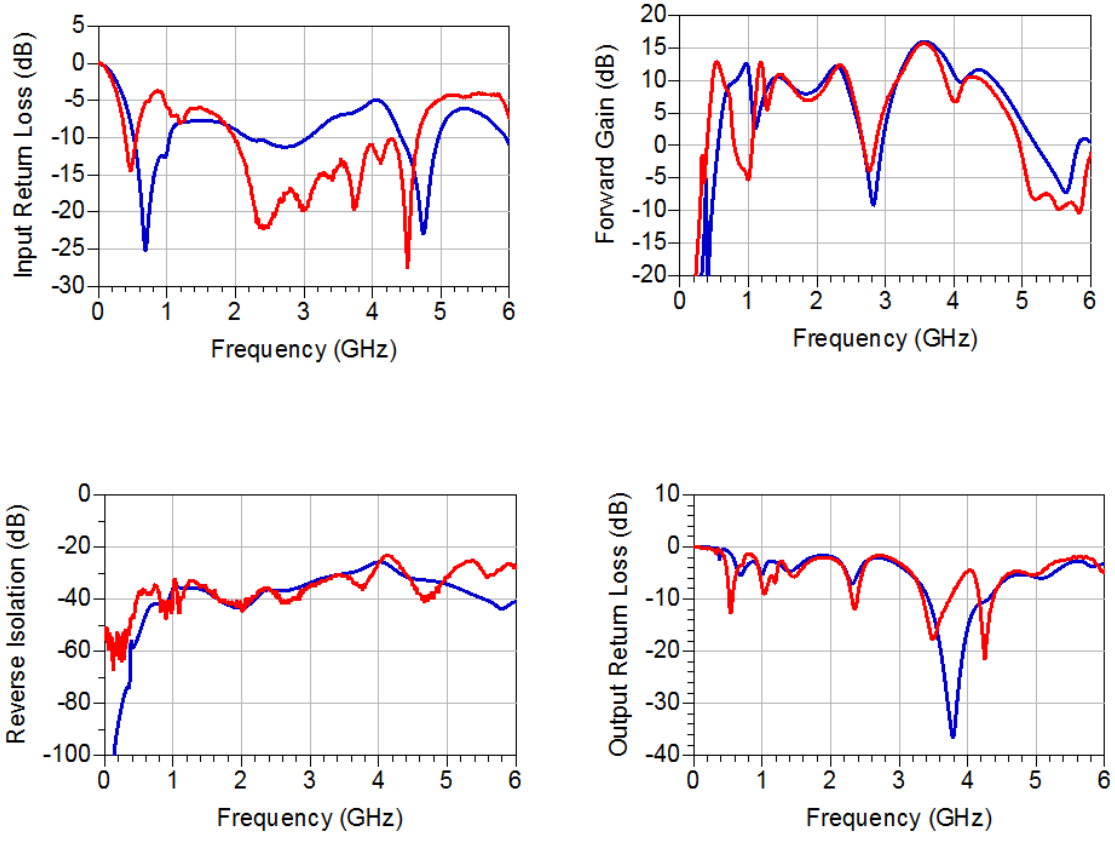


Figure 48: Simulated vs. Measured S-Parameters

The largest discrepancy between the simulated and measured small-signal results can be observed by the input return loss reported between 2 and 4 GHz. The measured results are approximately 5 dB better than those reported by simulated results. Additionally, the simulated output return loss is approximately 6 dB better than that reported by the measured results and can also affect the amplifiers performance characteristics. Many factors could attribute to this delta including part-to-part variation of passive and active components, phase inaccuracies into the recombining node, and dielectric substrate modeling.

The stability can be determined from the small-signal S-parameters discussed earlier from Rollet's condition defined by equation (2.3). The stability plot shown in Figure 49 shows that the device is unconditionally stable from approximately 2.3 to 4.2 GHz, which is adequate for the intended operation of this power amplifier. However, we can observe that the conditions for oscillations exist out of the intended band of operation. The use of a band-pass filter could be deployed to ensure that the out-of-band characteristics of the power amplifier are unconditionally stable, but would come at the cost of the filters insertion loss.

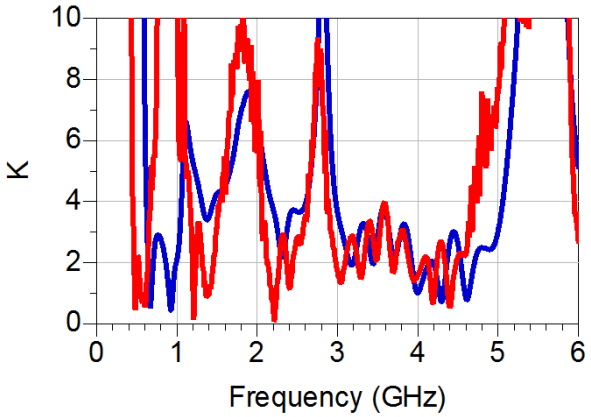


Figure 49: Simulated vs. Measured Stability (K)

From the forward gain plot shown in Figure 41 the bandwidth of the device can be ascertained and is provided in table 7. The calculated 1 dB percentage bandwidth of the 3.6 GHz Doherty power amplifier is approximately 7.8%. A limitation of the classical Doherty power amplifier's input configuration generally results in narrow bandwidth, but the results shown here are respectable, providing nearly 280 MHz of linear gain. The 2dB and 3dB frequency bandwidth and percentage bandwidths are also provided showing an increase to bandwidth as the insertion loss requirements in the passband are increased.

Table 7: Doherty PA Bandwidth

Insertion Loss (dB)	Lower Frequency (MHz)	Upper Frequency (MHz)	Frequency Bandwidth (MHz)	Percentage Bandwidth (%)
1 dB	3430	3710	280	7.78
2 dB	3365	3760	395	10.97
3 dB	3310	3800	490	13.61

5.4 Large-Signal Bench Calibration

A rigorous calibration process was required to remove any losses from the RF signal path so that the performance of the Doherty power amplifier could be tested and evaluated with high accuracy. A detailed description of the large-signal bench calibration process is provided in this section with accompanying figures to show the necessary steps required to accurately measure the 3.6 GHz Doherty power amplifier.

1. Power Meter/Sensor Calibration

   a. Set frequency 3.6 GHz

   b. Zero Power Sensor

   c. Calibrate Power Sensor

Figure 50: Power meter and sensor calibration

2. Subtract coaxial cable loss from the output of the ESG

   a. Use a THRU to connect the power sensor to the output of the ESG

   b. Apply a 0 dBm CW

   c. Apply an amplitude reference offset on the ESG so that a reading of 0 dBm is measured on the power meter.

Figure 51: Subtract coaxial cable loss

3. Subtract losses between the ESG output and DUT input

   a. Connect the output of the ESG to the input of the AR power amplifier

   b. Connect the output of the AR amplifier to the isolator.

   c. Connect the output of the isolator with a barrel connector

   d. Use a THRU to connect the power sensor to the barrel connector

   e. Adjust the gain on the AR amplifier until a 20dB a reading of 20 dBm is measured on the power meter.

   f. Apply an amplitude reference offset on the ESG

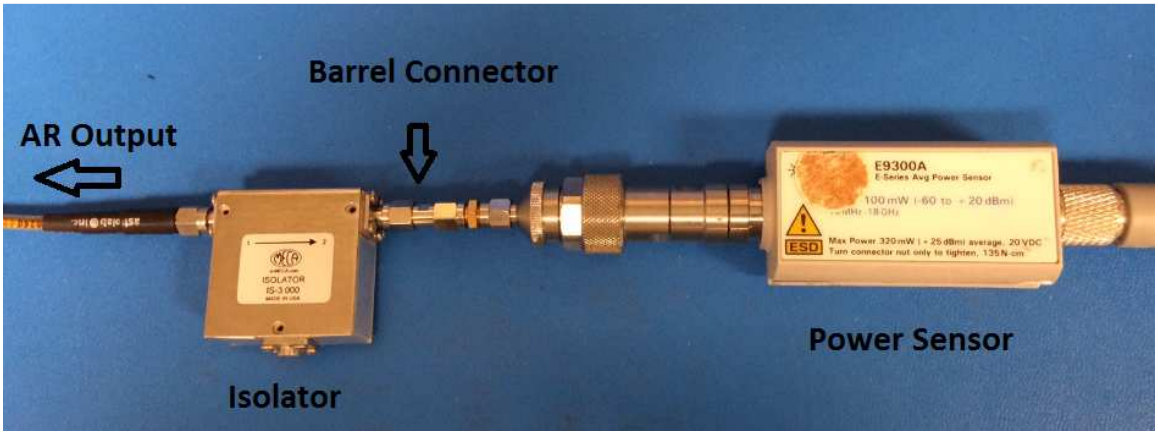


Figure 52: Subtract losses between ESG output and DUT input

4. Subtract losses through the 20 dB directional coupler

   a. Connect the barrel connector attached to the isolator to the input of the 20 dB directional coupler.

   b. Connect the 20 dB coupled port to the input of the signal analyzer

   c. Connect a 20 dB attenuator to the output of the directional coupler

   d. Connect the power sensor to the 20dB attenuator

e. Apply a 0 dBm CW from the ESG and set the reference level offset on the signal analyzer and power meter so that 0 dBm reading is reported from both instruments.

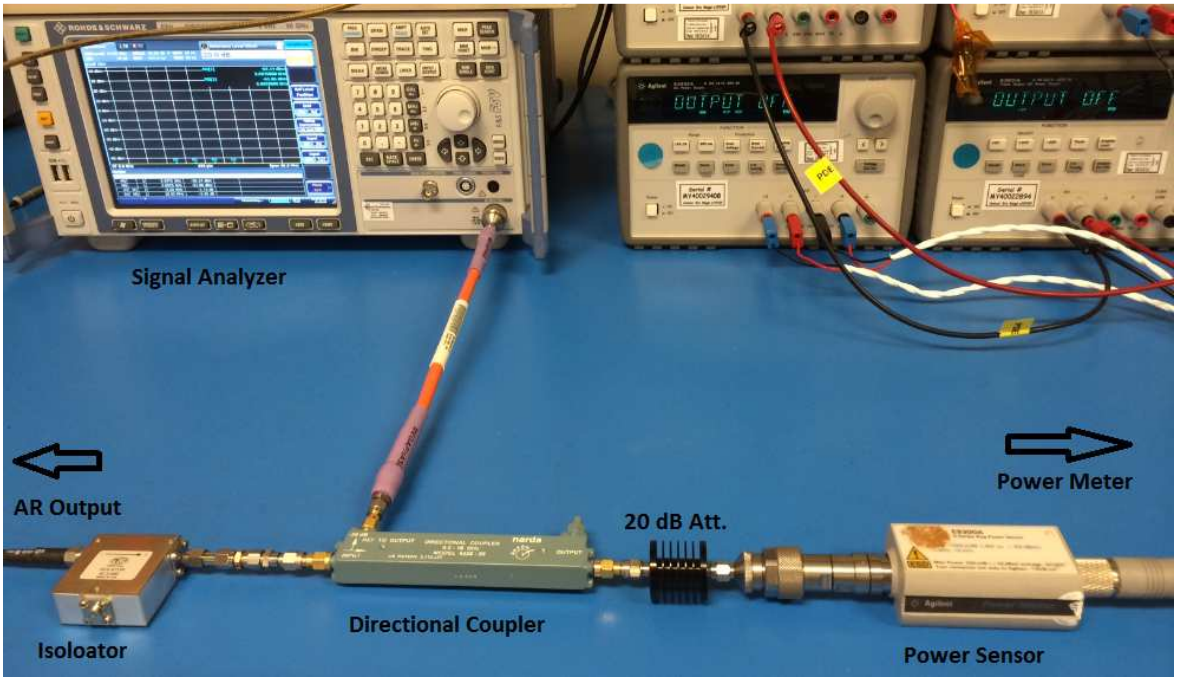


Figure 53: Subtract loss through directional coupler

A similar calibration procedure was performed for the two-tone IMD large-signal testing. Additional steps were necessary to calibrate the two-tone IMD large-signal bench where the power of each tone was set to produce equal outputs. The losses from each coaxial cable between the splitter and ESGs were accounted for by setting the amplitude reference offset on each individual ESG.

5.5 Single-Tone Large-Signal Tests

The measured single-tone large signal results were captured in 1 dB increments and compared with simulated results. Figure 54 shows that the measured results produced a maximum PAE of 55.1% and a PAE of 48.5% with

an input power backed-off by 6dB. Comparing these results with the simulated results reported a maximum PAE of 64.5% and a PAE of 50.4% with an input power backed-off by 6 dB. The measured maximum output power of 40.8 dBm was reported versus the simulated 41.7 dBm. This corresponds to a linear output power of 12 and 15 Watts respectively.

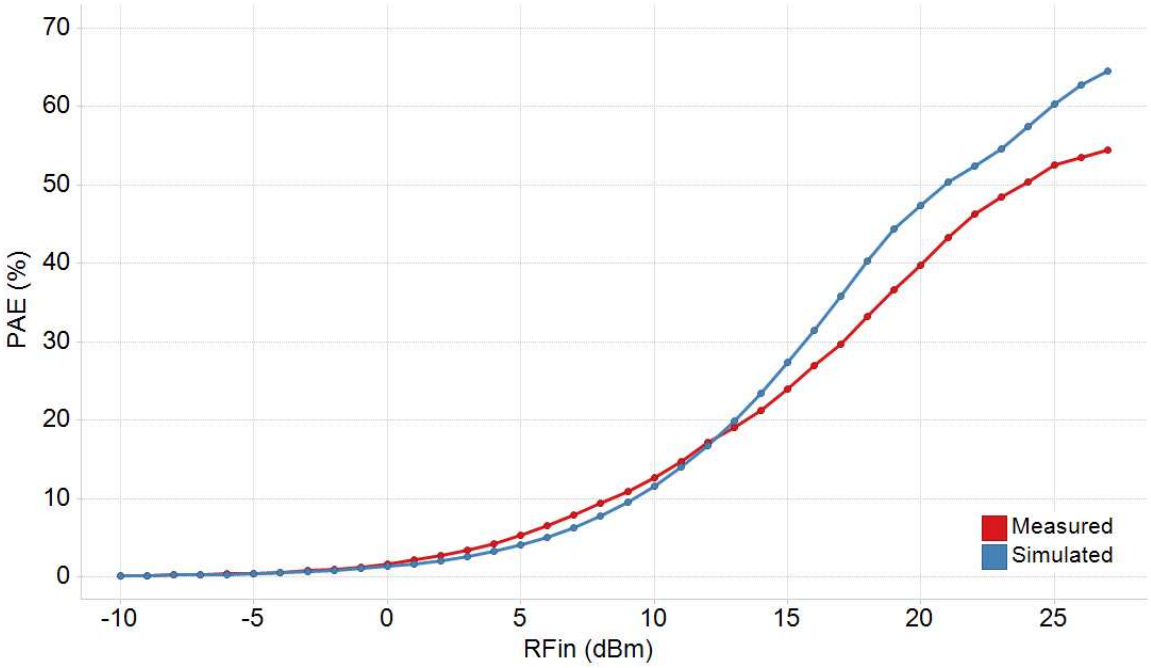


Figure 54: Measured vs. Simulated PAE (%)

Similarly, the transducer power gain was recorded in 1 dB increments by measuring the ratio of the power delivered to the load versus the power available from the source. Figure 55 shows the transducer power gain (dB) versus the RF output power (dBm). As the input power is increased we can observe the measured gain is decreasing. The decrease in measured transducer power gain versus that of the reported simulated results gives an explanation for the

discrepeancies between the reported PAE and maximum output power. Moreover, the 6dB delta measured between the S_{22} output return loss described in the S-parameter section demonstrates the effects that the output matching network has on PAE, maximum output power, and transducer power gain.

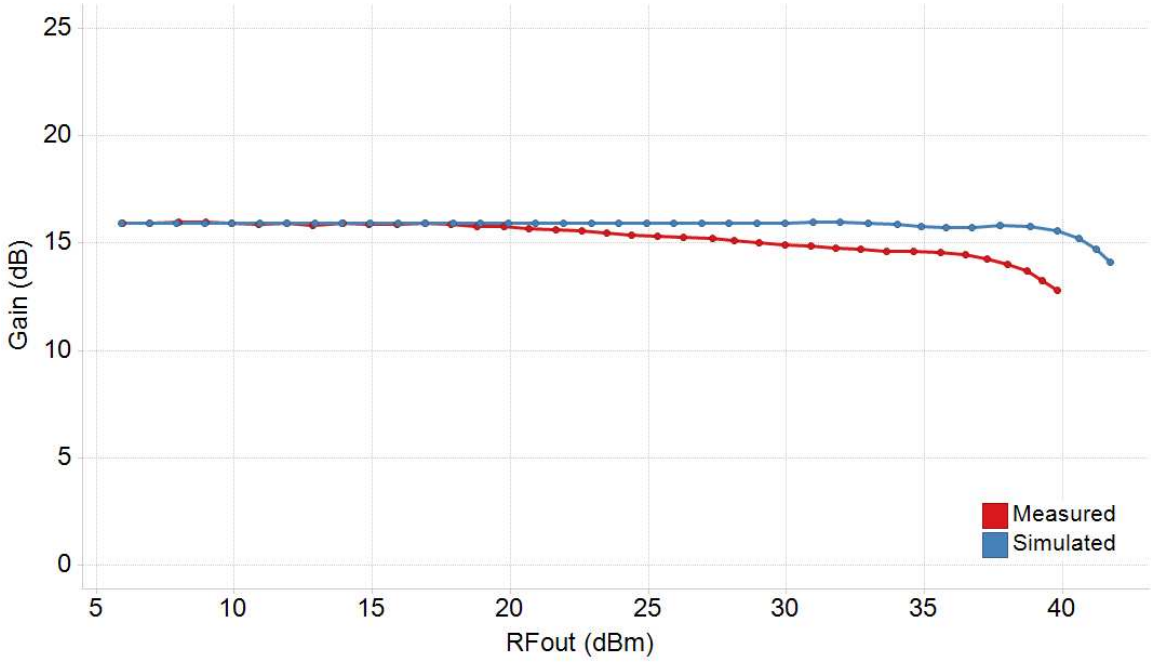


Figure 55: Measured vs. Simulated Transducer Power Gain (dB)

The 1 dB compression point can be found by extrapolating the linear gain curve beyond its measured saturation region and then determining the point where the measured gain is 1-dB below the extrapolated linear gain point. We can observe from the plot in Figure 56 that the linear extrapolation of the RF output power results in a 1 dB compression point of approximately 38.7 dBm. The simulated 1-dB compression could not be determined from the data provided but is approximated at 41 dBm.

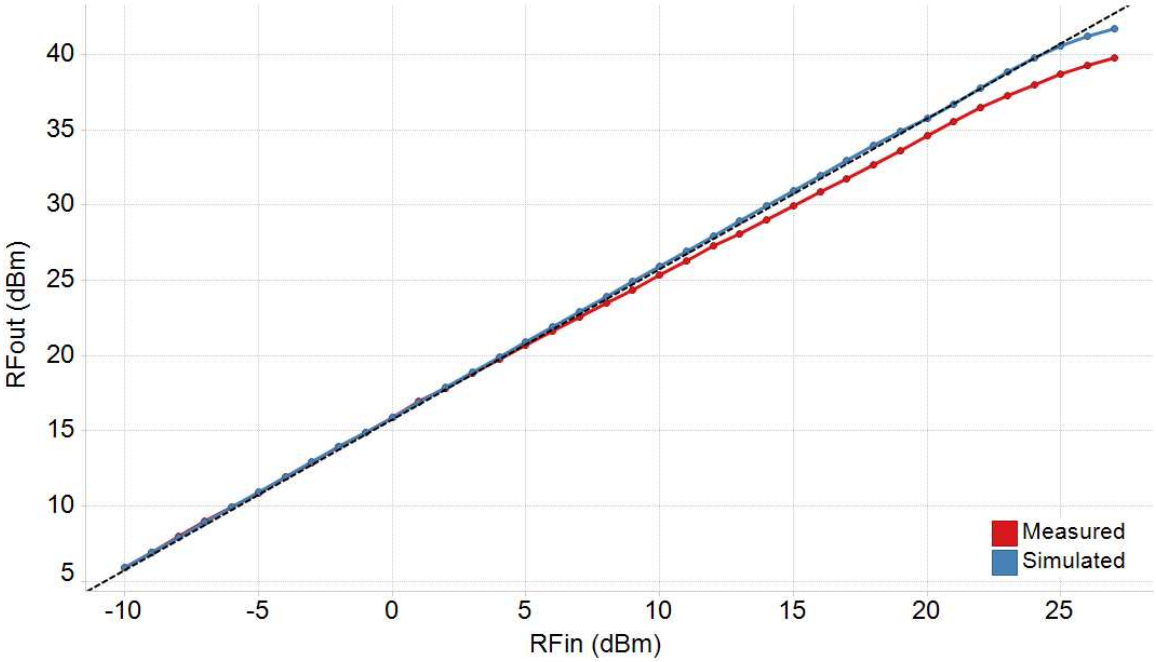


Figure 56: Measured vs. Simulated 1dB Compression Point (dB)

5.6 Large-Signal IMD Tests

The two-tone IMD large-signal results were measured to evaluate the linearity of the 3.6 GHz Doherty power amplifier. The tones were separated by 5 MHz which corresponds to a tone at 3597.5 MHz and 3602.5 MHz. This test is called out in IEEE IMS2014 student design competition for "High Efficiency Power Amplifier Design Competition," which evaluates the linearity of the power amplifier by requiring a carrier to intermodulation ratio greater than 30 dB. The input power will be incremented by 1dB from 0 dBm and the PAE will be measured at the first output power where the ratio falls below 30 dBc [26].

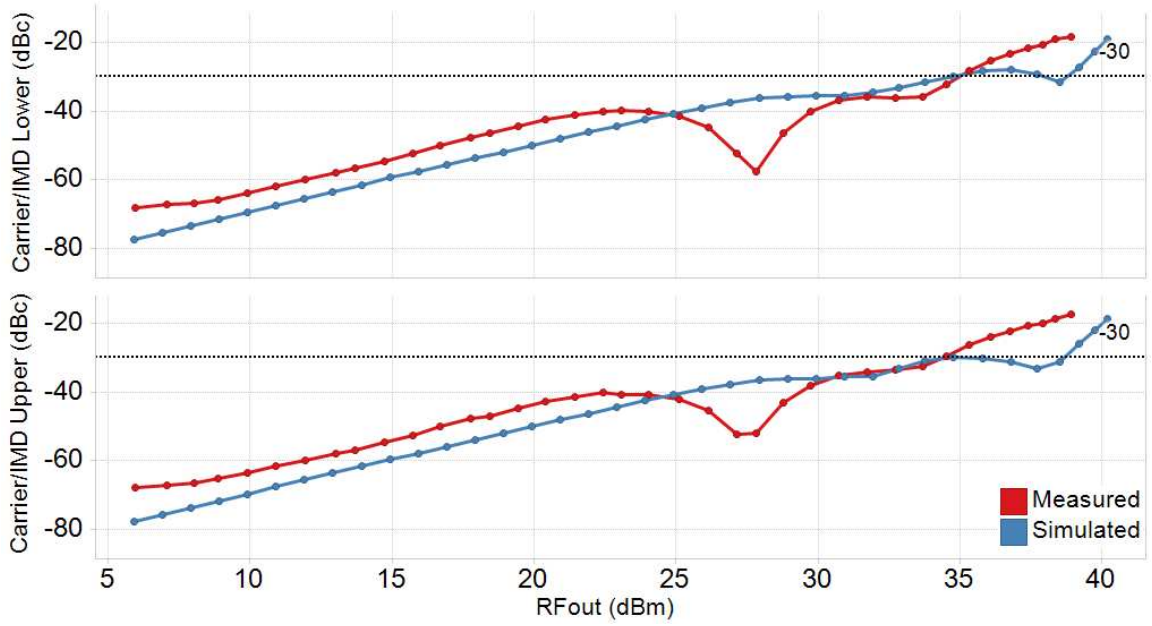


Figure 57: Simulated vs. Measured carrier to IMD ratio

Figure 57 shows the measured vs. simulated carrier to IMD ratio results. We can observe that the carrier to IMD ratio falls below the 30 dB carrier to IMD ratio with an input power corresponding to 20 dBm and an output power of 34.5 dBm. Figure 58 shows the two-tone PAE results of measured vs. simulated results. The PAE reported where the carrier to IMD ratio falls below 30 dB is 39.8%. This would result in a score of 54.8 which is determined by the product of the PAE and frequency weighting factor having the form $(GHz)^{0.25}$ [24]. The maximum measured two-tone PAE was recorded at 48.3% which is 10% lower than those reported simulated PAE. The two-tone transducer power gain reported similar values to those found in figure 55 and are not reported here for brevity. We may conclude that the delta created between the simulated and measured results is due to the deviation reported by the output return loss, amplifier biasing, and phase offsets in the input and output combining networks.

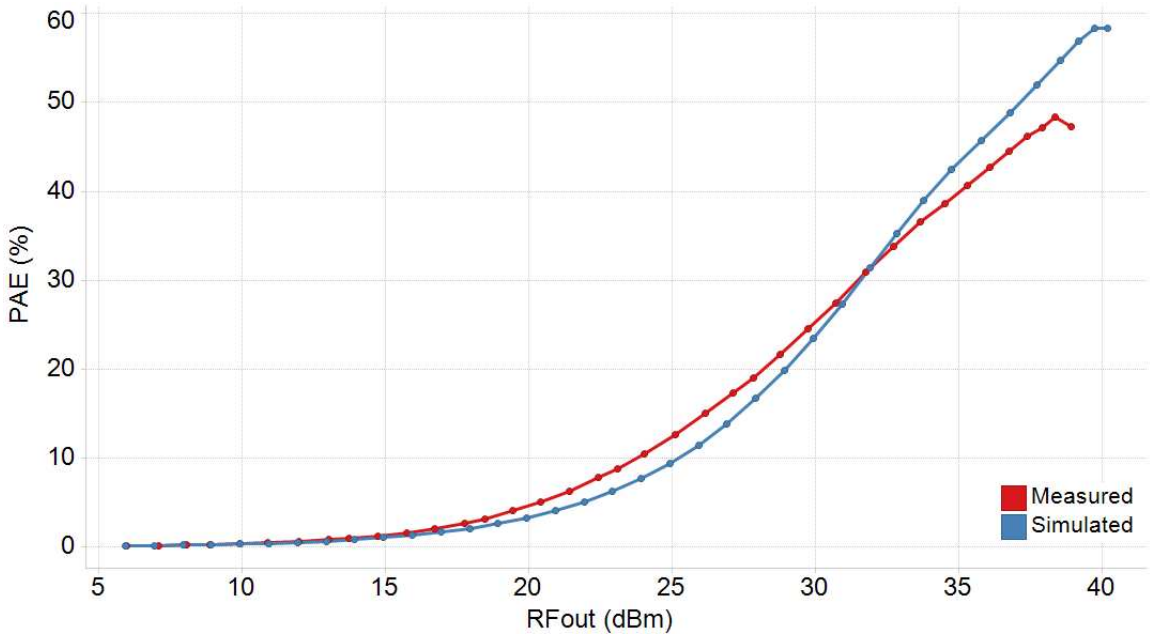


Figure 58: Measured vs. Simulated Two-Tone PAE (%)

Please observe the 3rd-order IMD improves between 25 and 30 dBm RF output power. Linearity sweet spots are a common phenomenon in traditional class AB power amplifiers. However, in a Doherty PA such cancellation effects become more prominent due to the interaction of main and peak amplifiers which have different bias points, thus different transfer characteristics [25]. A specific bias point can greatly improve the 3rd-order IMD but there are issues associated with it. First, tuning the quiescent current does not only affect the third order IMD but also the higher order IMDs. It happens in such a way that the 5th-order IMD becomes worse if the 3rd-order IMD improves [27]. This can be observed in Figure 59, where the 3rd-Order IMD improves resulting in degraded 5th-Order IMD. For obvious reasons, it is not practical to suppress 3rd-Order IMD products below 5th-Order IMD products.

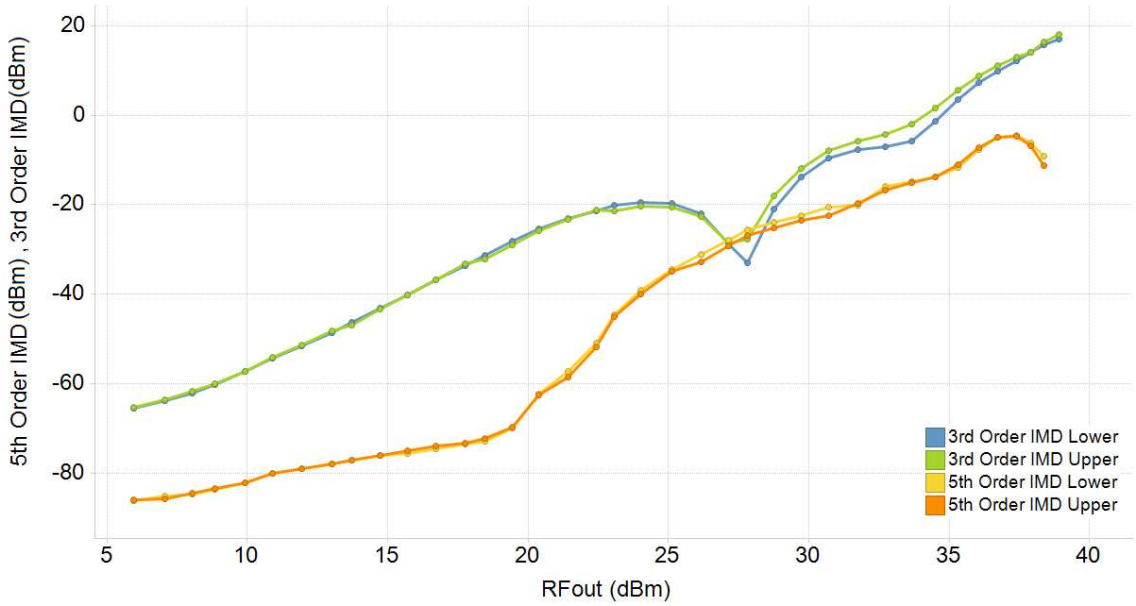


Figure 59: 3rd-Order and 5th-Order IMD

5.7 Large-Signal LTE Modulated Tests

The Doherty power amplifier can improve the efficiency of a PA when the input power is backed-off, making this architecture particularly attractive for high peak-to-average (PAR) environments. Demand for linear high efficiency power amplifiers in small-cell base station applications is required to support the increasing data rates for modulations such as Orthogonal Frequency Division Multiplexing (OFDM), which is used predominately in Long Term Evolution (LTE) 4G networks. Typically, the use of digital pre-distortion (DPD) is used to reduce the distortion mechanisms caused by AM-AM, AM-PM, and memory effects to achieve the linearity requirements of high PAR networks. This section will give the test results of the 3.6 GHz Doherty power amplifier when a 20 MHz LTE waveform is swept over RF output power. The results here are without the use of DPD, but if it were used we can expect that the distortion mechanisms caused

by AM-AM, AM-PM, and memory effects would be reduced, further improving the linearity of the power amplifier.

The modulated waveform is a quadrature phase shift keyed (QPSK) with a 20 MHz system bandwidth and an 18 MHz measurement bandwidth. This particular waveform uses all of its 100 resource blocks. An LTE resource block is defined as 12 contiguous subcarriers corresponding to 180 kHz in the frequency domain and one time slot in the time domain. The subcarriers in LTE have a constant frequency delta of 15 kHz. This means that in the frequency domain, one terminal can receive or transmit in one resource block or integer multiples of one resource block. In other words, it is not possible to assign less than 12 subcarriers to one terminal [29]

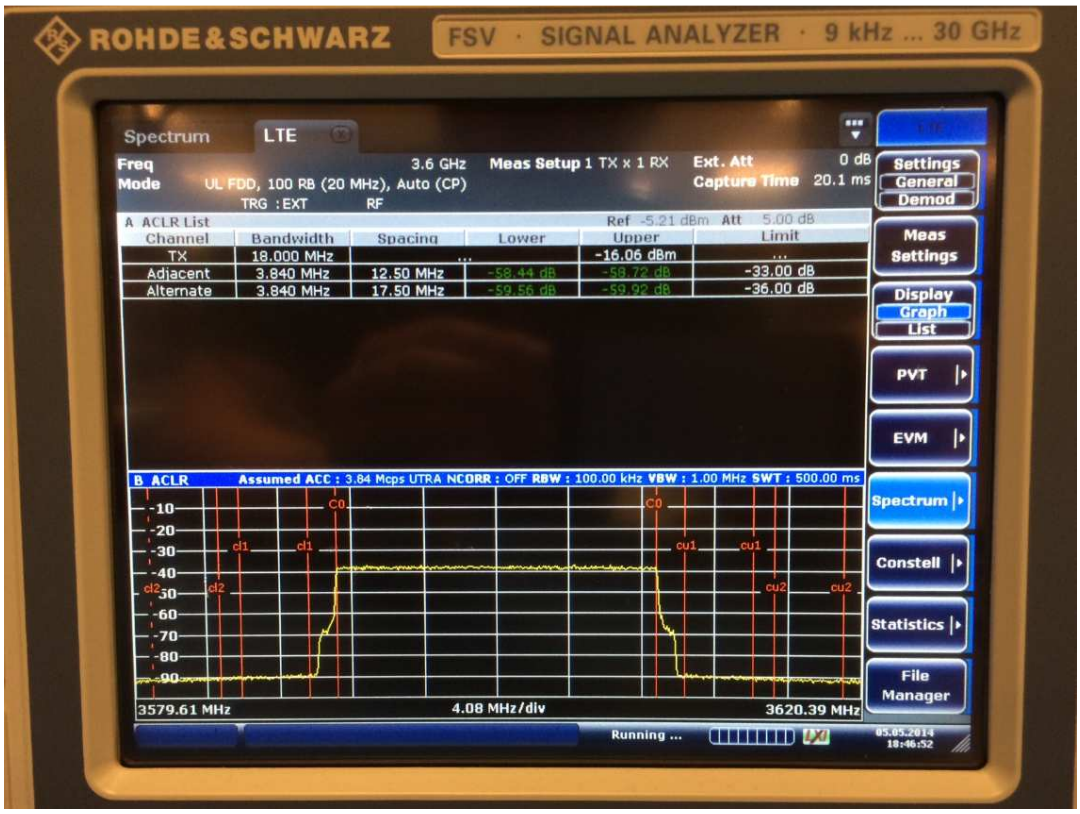


Figure 60: Measured PAE and Gain with 20 MHz LTE Waveform

The occupied bandwidth contains 99% of the total integrated mean power of the transmitted spectrum. The occupied bandwidth can be measured by performing spectral measurements with the Rohde & Schwarz FSV signal analyzer. Figure 61 shows the spectral emissions of the QPSK_20MHz_100RB test waveform. The adjacent channel leakage power ratio (ACLR) is an important measure to verify that the transmitter does not cause unacceptable interference to an adjacent channel. In 4G networks the ACLR must be verified for two different scenarios which are distinguished by EUTRA and UTRA spectral emissions. The example provided in Figure 61 shows the EUTRA ACLR where it is assumed that the adjacent channel is another LTE channel. We can observe that as the input power is swept in 1 dB increments the ACLR begins to degrade after output power approaches 27 dBm, and fails the EUTRA ACLR specification limit of -30 dBc at approximately 35 dBm

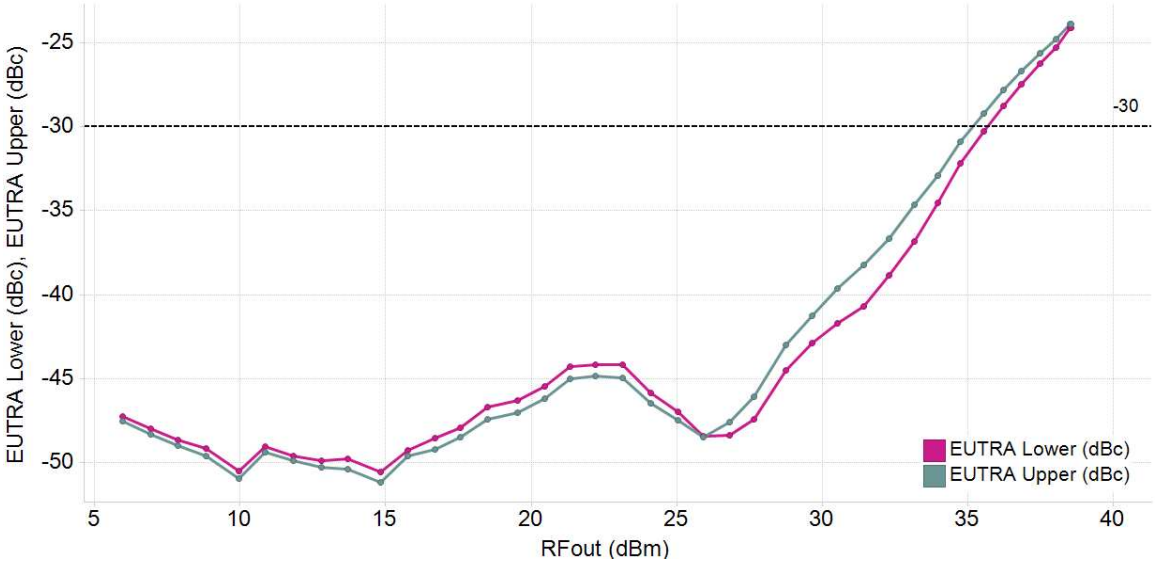


Figure 61: EUTRA-ACLR (dBc) vs RF Output Power (dBm)

Conversely, the UTRA measurement would treat the adjacent channel measurement as if it were being utilized by a WCDMA channel and calls out a more stringent ACLR specification of -33 dBc. The ACLR results reported in Figure 61 demonstrates that the 3.6 GHz Doherty power amplifier can support a 20 MHz LTE network up to an output power of 35 dBm without the use of DPD. Dynamic memory effects must be compensated for using DPD to improve the linearity of the device beyond an output power of 35 dBm. In GaN HEMT devices these memory effects are predominately caused by the effects of trapping [7].

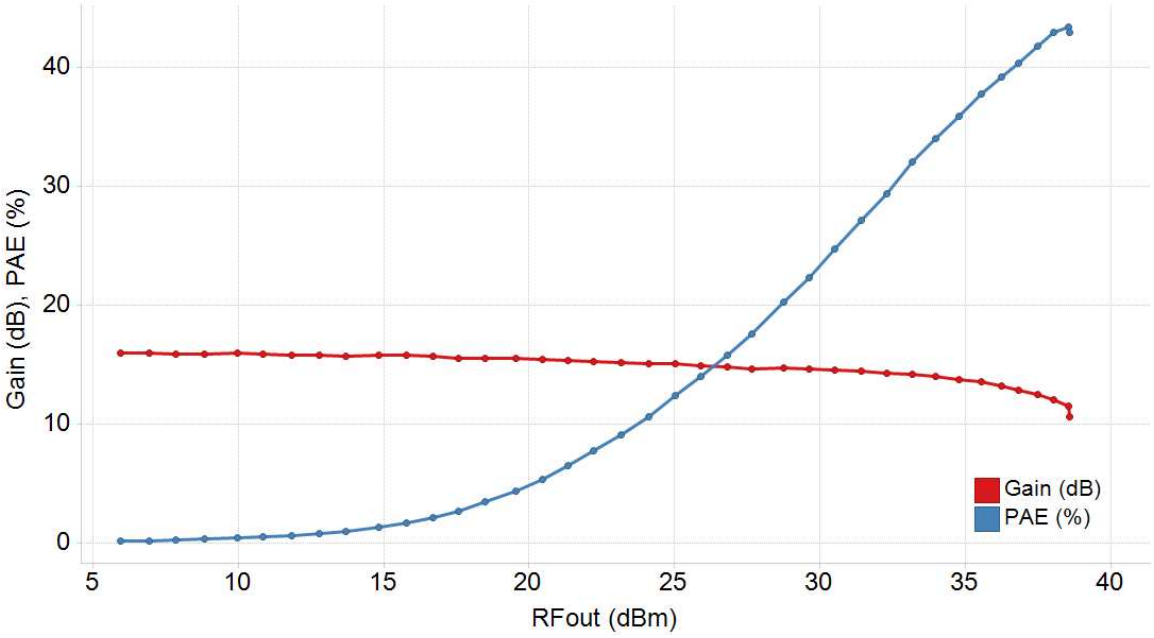


Figure 62: Measured PAE and Gain with 20 MHz LTE Waveform

The transducer power gain and PAE efficiency are reported in Figure 62 using the modulated 20 MHz LTE waveform. The maximum PAE reported was 43.4% and with the input power backed-off by 6dB the PAE is equal to 37.82% and corresponds to an output power of 35.6 dBm. The maximum output power

measured is 38.6 dBm, which is less than the maximum output power reported for single-tone and two-tone measurements. This is an expected outcome because as you increase the bandwidth of a power amplifier with a modulated waveform, the power spectral density will decrease, resulting in a lower maximum output power.

5.8 Thermal Imaging Results

The Flir T650sc was used to capture the thermal images shown in Figure 63, where the amplifier was driven to full saturation to a maximum output power of 40.8 dBm [30]. The camera has a feature that enables it to focus on a specific area and report the temperature which allowed us to focus on the individual T1G6001032-SM GaN devices to report their operating temperature at maximum output power. We can observe that the carrier amplifier (left) is 2.5℃ warmer than the temperature reported by the peaking amplifier (right). This agrees with our expectations since the majority of the power is being dissipated by the carrier amplifier. The temperature ranges from 26.5℃ to 4 4.2℃ where the top metal layer maintains a temperature just above the ambient room temperature, demonstrating the effectiveness of the 4” x 4” aluminum heat sink.

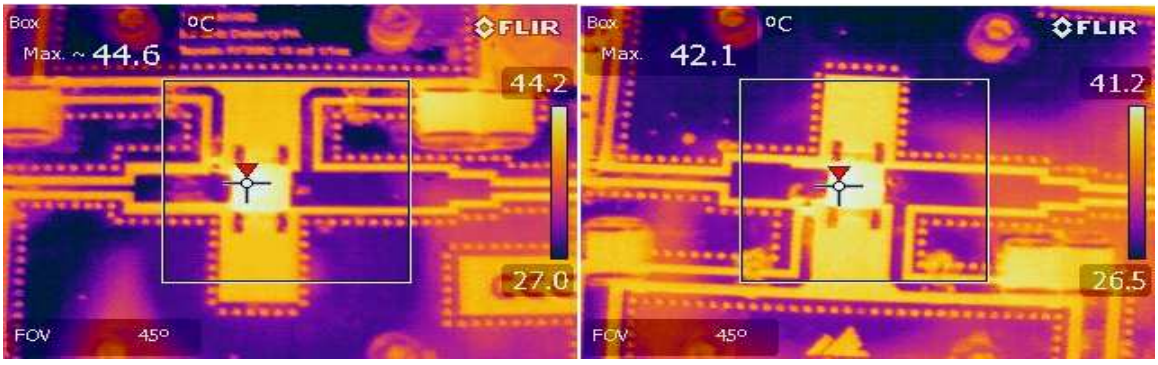


Figure 63: Thermal Image of Carrier (Left) and Peaking (Right)

Chapter 6
Discussion, Conclusions, Future Work, and Closing Remarks

6.1 Discussion

The Doherty power amplifier was first introduced in 1936 and has seen a recent resurgence in popularity due to the potential efficiency improvements for modulation schemes possessing high peak-to-average ratios like those used in 4G LTE networks. The design trade-off of high efficiency usually comes at the cost of degraded linearity and the Doherty power amplifier is no different. The work presented here describes an active load modulated amplifier, with an input and output network tuned to achieve high linearity, thereby trading-off its maximum PAE and backed-off PAE. The load modulation characteristic is much softer than in an ideal, symmetric Doherty power amplifier, which implies that the carrier amplifiers drain voltage is not saturated at the onset of load modulation.

The motivation for this project was to evaluate the active models created by Modelithics. The third-party modeling vendor recently partnered with TriQuint to model TriQuint's 2nd generation GaN HEMT devices. To the knowledge of this author this is the first Doherty power amplifier developed using these active device models. The simulated and measured results of the 3.6 GHz Doherty power amplifier reflected positively on the use of these active device models and demonstrated a functional first-pass design without the use of classical load-pull analysis. This represents a benchmark in TriQuint device modeling which has predominately relied on load-pull analysis for its production line of GaN power amplifiers [29].

6.2 Conclusions

This manuscript described the design, development, and implementation of a 3.6 GHz Doherty power amplifier with a saturated output power of 40 dBm, using TriQuint's 2nd Generation GaN on SiC HEMT devices (T1G6001032-SM). Advanced Design Systems (ADS) simulation software, in conjunction with Modelithic's active and passive device models, were used to model the design throughout each step of the design process. The use of these device models demonstrated a successful first-pass design and a comparison of the simulated and measured results were reported. The omission of classical load-pull analysis represents a potential reduction in design-cycle times, enabling a design team to get their product to market faster.

The realized 3.6 GHz Doherty power amplifier had a maximum PAE of 55.1% and reported a PAE of 48.5% when the input power was backed-off by 6dB. A maximum output power of 40.8 dBm was achieved while excited by a single-tone at 3.6 GHz. Conversely, when a 20 MHz LTE waveform was used to evaluate the performance of the Doherty power amplifier, a maximum output power of 38.6 dBm was attained. This degradation to the maximum output power can be explained using elementary systems and signal analysis, where if the bandwidth of a system is increased, the power spectral density will decrease. The two-tone IMD test demonstrated the load modulated amplifiers linearity versus output power and meets the -30 dBc design criteria up to an output power of 34.5 dBm, corresponding to a PAE of 39.8%. The 3rd -order IMD characteristics shows a linearity improvement between 25 and 30 dBm and can

be attributed to the cancellation effects due to the interaction between the carrier and peaking amplifiers where the separate bias points creates the individual transfer functions resulting in the cancellation of 3rd-order IMD products.

6.3 Future Work

Continued efforts leading up to IMS2014 are in order to determine the optimal bias point of the 3.6 GHz Doherty power amplifier. It's advantageous to determine the bias point where the 3rd-order and 5th-order IMD products simultaneously reach the -30 dBc design specification. This would fully exploit the cancellation effects of the IMD products in an effort to return a more favorable PAE, resulting in a higher FOM for the competition.

The future work of this design hinges on the availability of the active GaN HEMT devices (T1G6001032-SM). The active devices are currently out of stock in TriQuint's inventory and the six samples provided to this author were exhausted during the evaluation and testing of the Doherty power amplifier. Most of which were damaged during the evaluation period, because the turn-on and shut-down protocol sequence was not strictly followed. These devices have not been officially released to the public, but we are hopeful that requests for additional samples will be provided.

A continued effort tuning the phase of the input and output combining network is necessary to optimize the performance of the Doherty power amplifier. Please recall that tuning handles were added to the output combining networks of the carrier and peaking amplifier to ensure that the phase is recombining equally. However, all but one of the PCBs were exhausted during the assembly

and evaluation phase of this project and with no parts currently available this author is reluctant to modify the only existing functional hardware.

6.4 Closing Remarks

While working on the thesis project described within this manuscript, the author was introduced to many new aspects of microwave design, technology, and methodologies. This project can be highlighted by unique milestones that are provided in the bulleted notes below, and represent ‘first-time’ exposure to such.

- RF Amplifier design using GaN
- RF Amplifier design above 26 dBm
- RF Amplifier design above 1.0 GHz
- Load Modulated Power Amplifiers
- Hot-Plate Assembly Techniques

A good thesis project challenges a student to reach to the limits of their abilities and aptitude. This thesis project has provided an outlet for personal development and adds to a growing project portfolio after completing the MS curriculum at Portland State University. The reward for these academic pursuits will ultimately be measured in the accomplishments of this author in the months and years following a public thesis defense. The inspiration to design an active load modulated amplifier began several years ago. With the results presented in this manuscript provides the forward momentum to transition into the next project has materialized.

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